

Model Name : Scala\_CAS/Kamiq\_CAS GN20E  
Compal Project Name : GH53Z  
File Name : LA-L031P

# Compal LA-L031P

## GH53Z MB Schematics Document

AMD Cezanne (FP6) Platform

REV : 1A

2020-01-04

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Power Plane	Description	S0	S3	S5
+19V_VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_SOC	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.75VALW	0.75V always on power rail	ON	ON	OFF
+0.75VS	0.75V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for APU and DDR	ON	ON	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+MEM_VDDQ	1.1V/0.6V switched power rail for LPDDR4/4x	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	AC-ON DC-OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+TP_VCC	3.3V Touch Pad power	ON	ON	OFF
+TS_PWR	3.3V Touch Screen Power	ON	ON	OFF
+FP_VCC	3.3V Finger Print power	ON	ON	OFF

Master	Device	Address[7:1]	Address [7:0]	
			Write	Read
I2C Port 0 (+1.8VS)	Touch Screen (Reserve)			
I2C Port 1 (+1.8VS)				
I2C Port 2 (+3VS)				
SBMUS Port 0 (+3VS)	JDIMM1	0101 0000b 50h	1010 0000b A0h	1010 0001b A1h
	JDIMM2	0101 0001b 51h	1010 0010b A2h	1010 0011b A3h
I2C_3_SCL (+3VALW)	PTP (Synaptics)	0010 1100b 2Ch	0101 1000b 58h	0101 1001b 59h
	PTP (ELAN)	0001 1111b 15h	0011 1110b 3Eh	0011 1111b 3Fh
SMBus Port 1 (+3VALW)				

EC_SMB_CK1 (+EC_VCC)	Smart Battery	0000 1011b 0Bh	0001 0110b 16h	0001 0111b 17h
	Charger IC	0000 1001b 09h	0001 0010b 12h	0001 0011b 13h
EC_SMB_CK2 (+EC_VCC)	APU Temp.	0100 1100b 4Ch	1001 1000b 98h	1001 1001b 99h
	GPU Temp.	1001 1110b 9Eh		
	Thermal Sensor Temp. (UF1)	1001 101xb		
	Thermal Sensor Temp. (UF2)	1001 0000b 90h		
EC_SMB_CK3 (+5VS)	RGB KB Driver IC	1100 0000b C0h		
ESB_CLK (+EC_VCC)	KC3810	1100 0000b C0h		

Board ID	PCB Revision
0	Rev 0.1
1	Rev 1.0
2	
3	
4	Rev 0.1 + RGB KB
5	Rev 1.0 + RGB KB
6	
7	

[illegible]

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

The timing diagram illustrates the sequence of power-up events for the 100-pin package. The signals are organized into four groups: G-A, G-B, G-C, and G-D. Each group contains multiple signals that are activated in a specific order, as indicated by the rising edges of the waveforms.

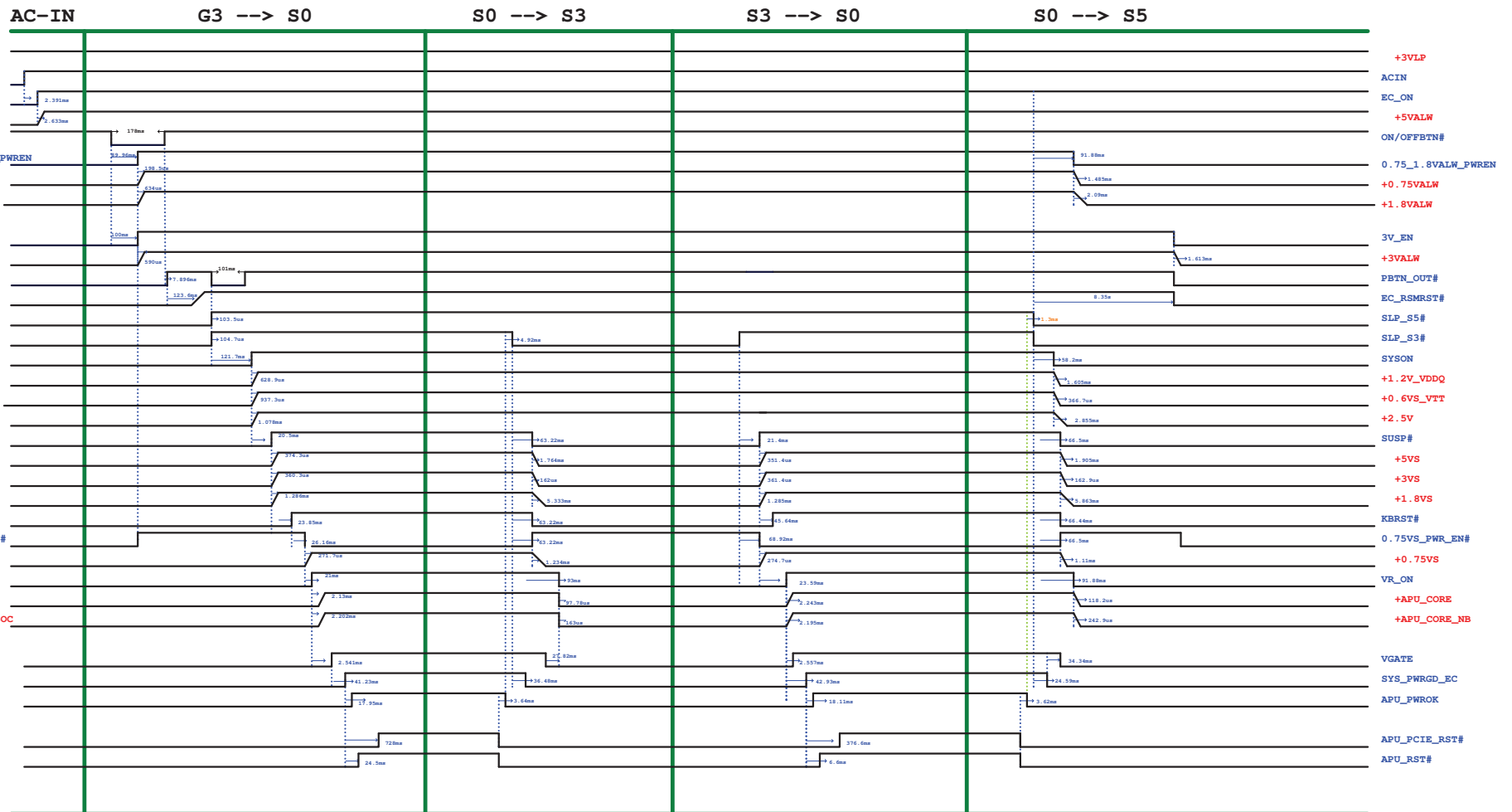
- G-A:**
  - +RTCBATT
  - EC\_ON
  - +5VALW
- G-B:**
  - 0.75\_1.8VALW\_PWREN
  - +1.8VALW/+0.75VALW
  - 3V\_EN
  - +3VALW
- G-C:**
  - SYSON
  - +1.2V/+2.5V
  - SUSP#
  - +5VS/+3VS/+1.8VS/+MEM\_VDDQ
  - 0.75VS\_PWR\_EN#
  - +0.75VS
- G-D:**
  - VR\_ON
  - +APU\_CORE
  - +APU\_CORE\_SOC

The diagram shows that the power-up sequence starts with G-A, followed by G-B, then G-C, and finally G-D. The signals within each group are activated in a specific order, with some signals (like +5VALW and +3VALW) being active for a longer duration than others.

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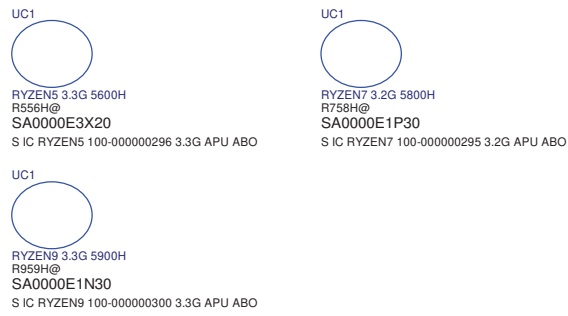
Power Sequence



Main Func = CPU

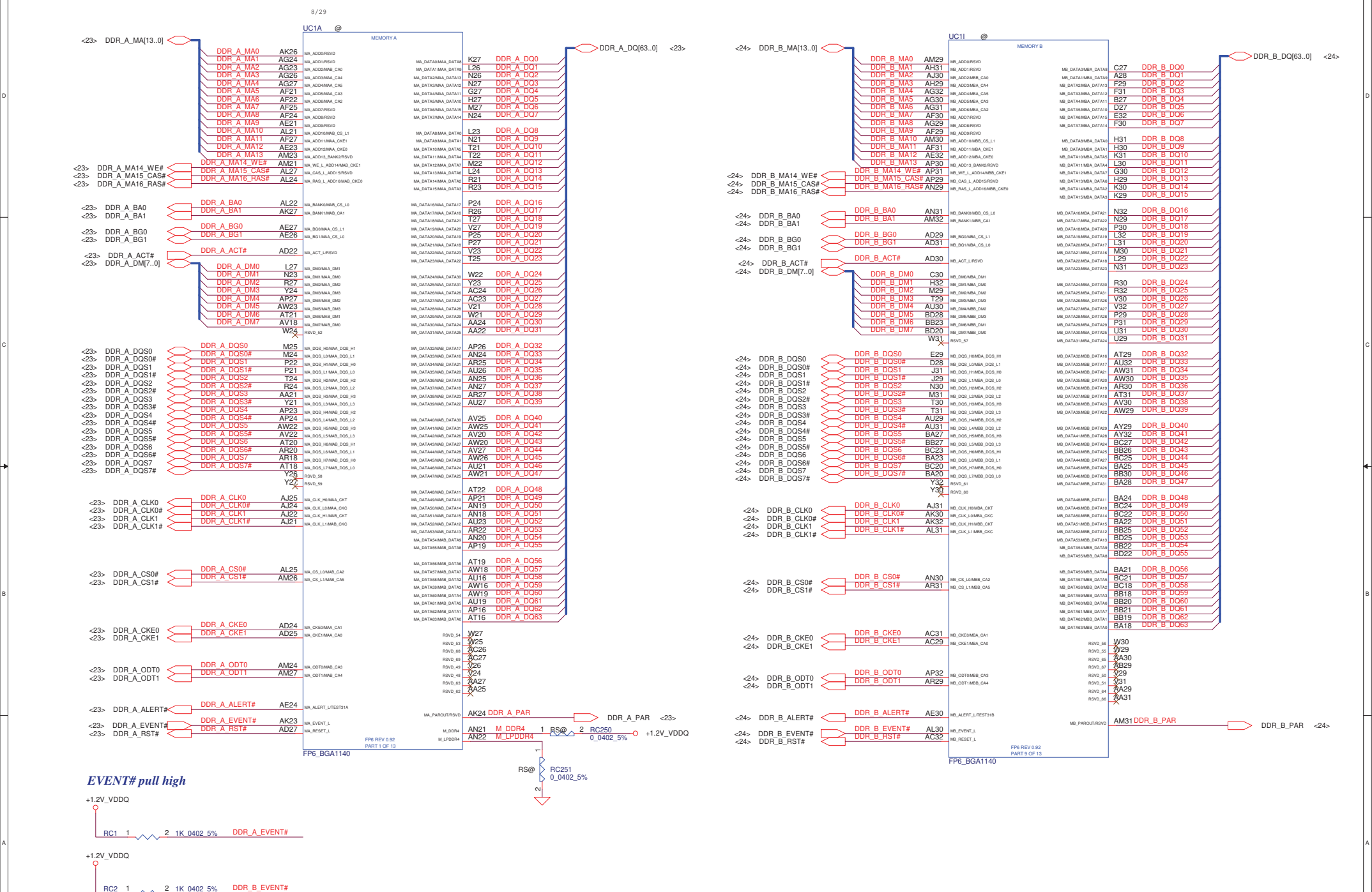


APU PN Table

	<p>RYZEN5 3.3G 5600H R558H@ SA0000E3X20 S I C RYZEN5 100-000000296 3.3G APU ABO</p> <p>RYZEN7 3.2G 5800H R758H@ SA0000E1P30 S I C RYZEN7 100-000000295 3.2G APU ABO</p> <p>RYZEN9 3.3G 5900H R959H@ SA0000E1N30 S I C RYZEN9 100-000000300 3.3G APU ABO</p>
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Main Func = CPU





## SVID

Diagram illustrating the SVID (Serial Voltage Identification) pin configuration. The pins are connected to a +1.8VSWLW supply. The configuration is as follows:

Pin	Value	Resistance	Label
RC109	1	2 1K 0201 5%	SVT_PWR_APU_R
RC110	1	2 1K 0201 5%	SVC_PWR_APU
RC111	1	2 1K 0201 5%	SVD_PWR_APU

Timing diagram for APU signals:

- APU\_TCK: RH34 1, 2 1K 0402 5%
- APU\_TMS: RH35 1, 2 1K 0402 5%
- APU\_TDI: RH36 1, 2 1K 0402 5%
- APU\_DBREQ#: RH37 1, 2 1K 0402 5%
- APU\_TRST#: RH26 1, 2 1K 0402 5%

A vertical red line on the right is labeled +1.8VALW.

**Figure 10: eDP DP Out Driver Schematic**

The schematic illustrates the output drivers for the eDP DP Out pins. It consists of three main sections, each showing an op-amp (UC66, UC64, UC65) configured as a voltage follower, driven by a resistor divider network.

- ENBKL Driver:** The input `ENBKL_R` is connected to a resistor divider (2.47K and 2.10K) which is also connected to `+1.8VALW`. The output of the divider is connected to the non-inverting input of UC66. The output of UC66 is `ENBKL`, which is connected to the `ENBKL` pin of the eDP DP Out.
- ENVDD Driver:** The input `ENVDD_R` is connected to a resistor divider (2.10K and 2.10K) which is also connected to `+1.8VALW`. The output of the divider is connected to the non-inverting input of UC64. The output of UC64 is `ENVDD`, which is connected to the `ENVDD` pin of the eDP DP Out.
- INVTPWM Driver:** The input `INVTPWM_R` is connected to a resistor divider (2.10K and 2.10K) which is also connected to `+1.8VALW`. The output of the divider is connected to the non-inverting input of UC65. The output of UC65 is `INVTPWM`, which is connected to the `INVTPWM` pin of the eDP DP Out.

The schematic is labeled **FH51S** and **Downsize for eDP routing**.

DP\_STEREO SYNC

RC1551 2 K 0402 5%

RC1541 2 K 0402 5%

+1.8VS

RC112 1 10K 0201 5%

RC113 1 10K 0201 5%

RC114 1 10K 0201 5%

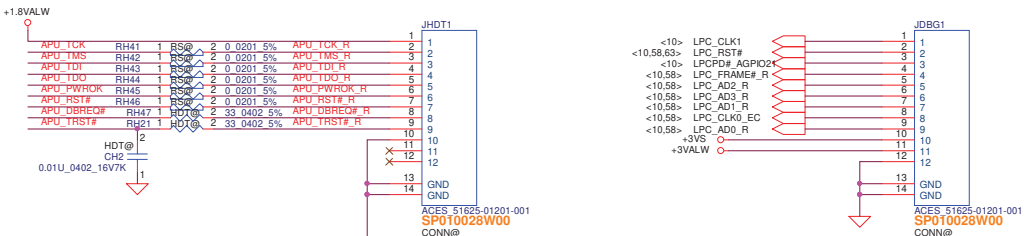
RC115 1 10K 0201 5%

APU\_TEST14

APU\_TEST15

APU\_TEST16

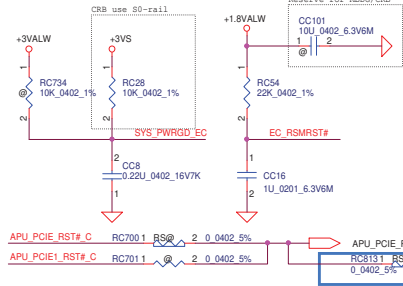
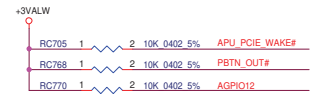
APU\_TEST17



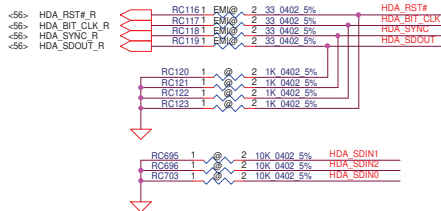
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## ACPI

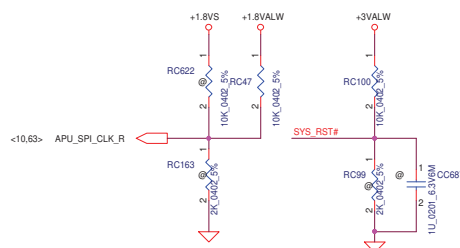


## HDA

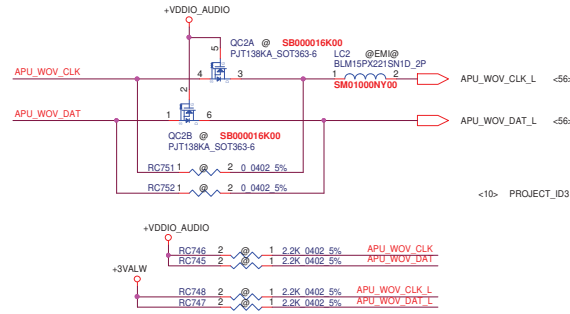


## Strap Pin

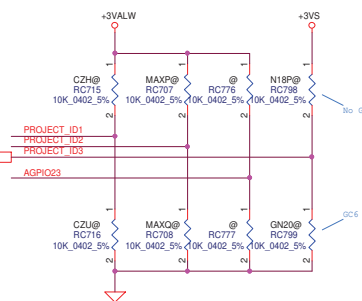
	APU_SPI_CLK_R	SYS_RST#
H	USE 48MHz CRYSTAL (Default)	NORMAL RESET MODE (Default)
L	USE 100MHz PCIe CLOCK AS REFERENCE CLOCK	SHORT RESET MODE



## APU WOV (Reserve)

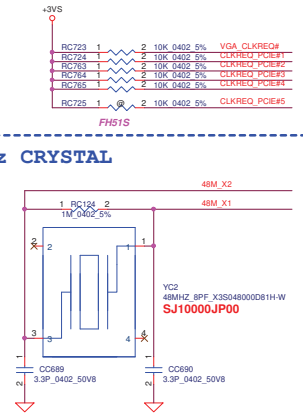


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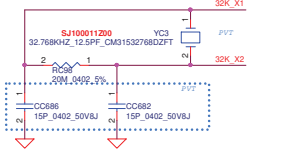


	Project_ID1 (AGP1010)	Project_ID2 (AGP1011)	AGP1023	Project_ID3 (AGP1014)
H	Cezanne-H	MAX-P GPU	Gaming_series	N18P GC6_no-support
L	Cezanne-U	MAX-Q GPU	Aspire 7	GN20 GC6_support

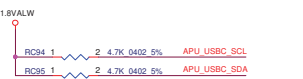
48MHz CRYSTAL



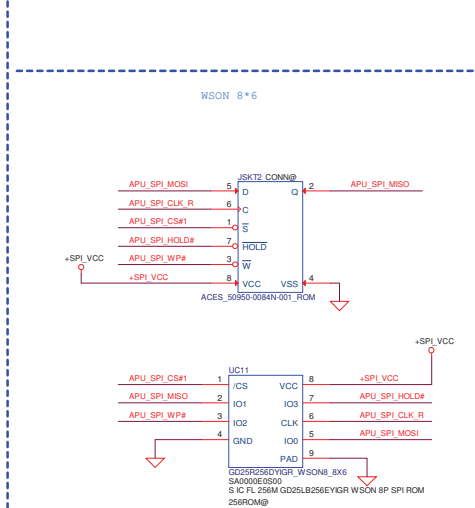
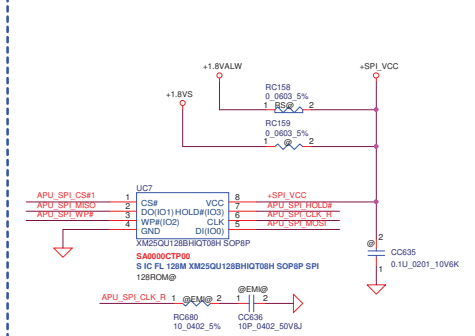
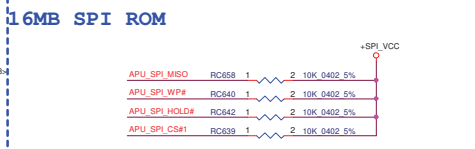
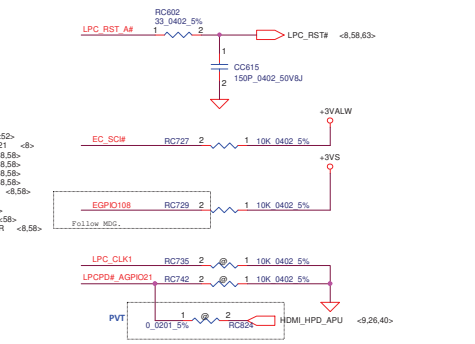
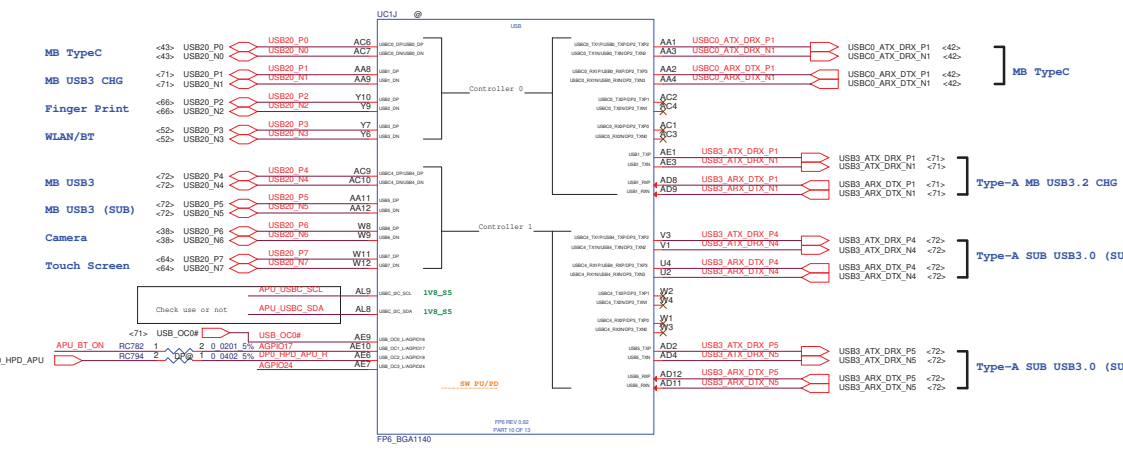
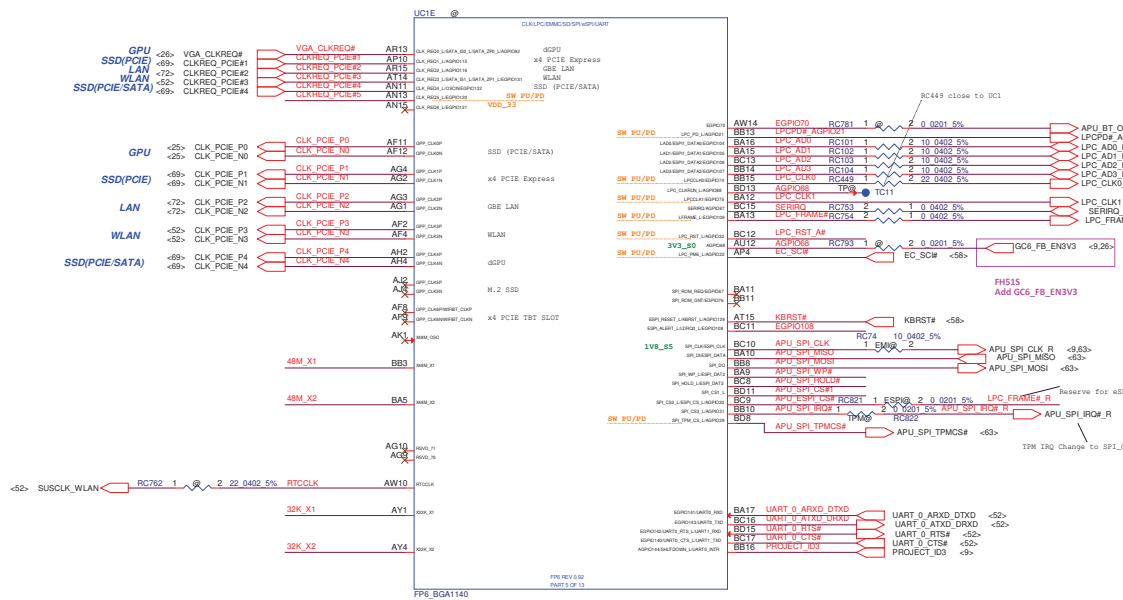
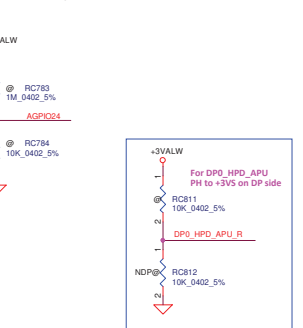
32.768KHz CRYSTAL



USB Function



Reserve



## Main Func = CPU

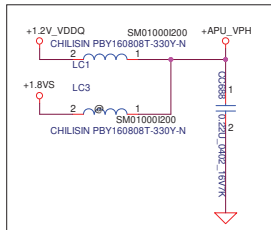
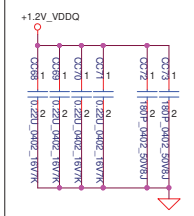
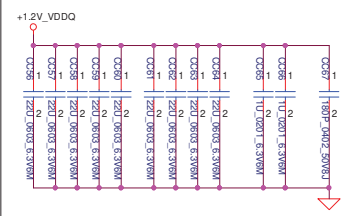
```
+APU_CORE_SOC Cap
place at Power Side
```

SCL/MBDG:  
7\*22uF (BU)  
1\*1uF (BU)  
1\*180pF (BU)

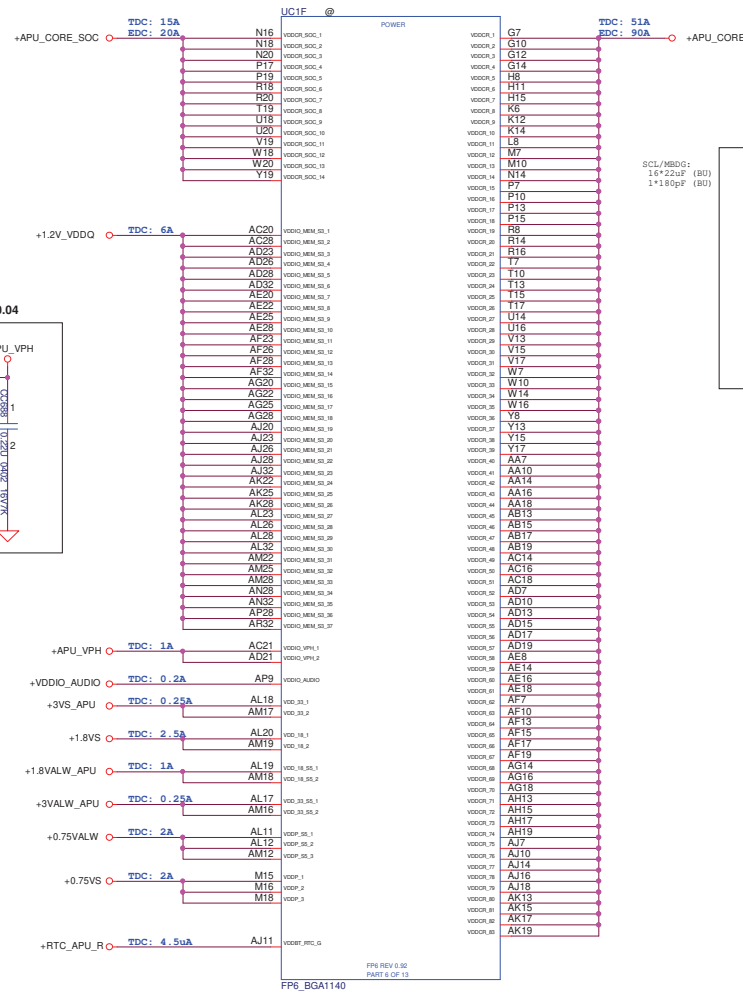
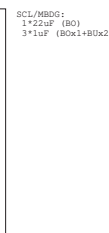
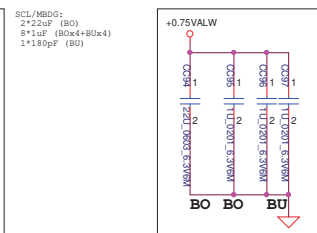
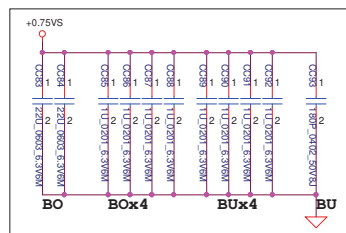
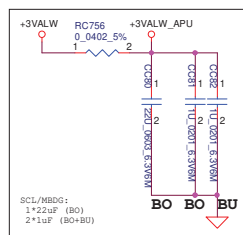
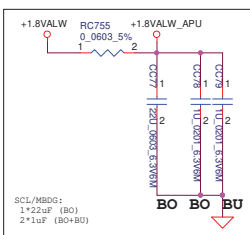
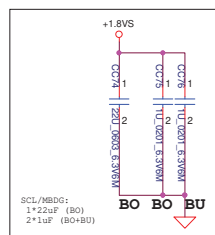
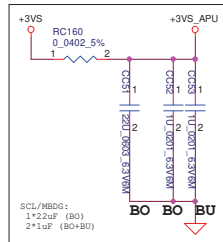
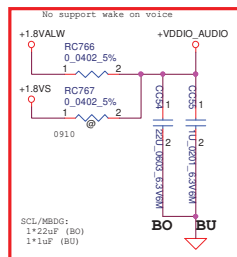
teknisi-indonesia

SCL/MBDG:  
7\*22uF (BU)  
2\*1uF (BU)  
4\*0.22uF  
1\*180pF (BU)  
2\*180pF

SM01000I200  
3000ma 33ohm@100mhz DCR 0.04

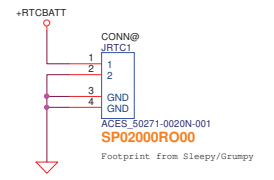
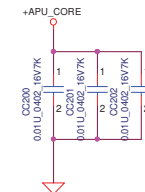


All BU(on bottom side under SOC) **ACROSS VDDIO AND VSS SPLIT**

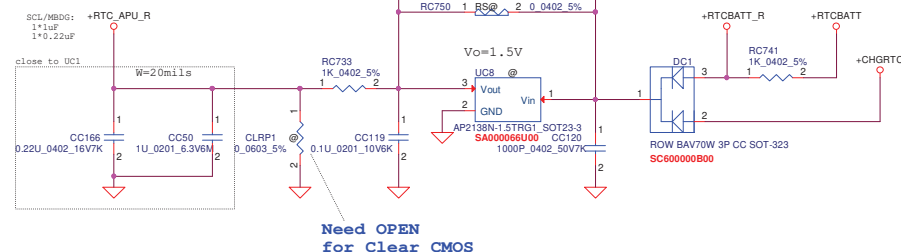


```
+APU_CORE Cap place at Power Side
```

### Stitching Cap.



## RTC OF APU



Need OPEN  
for Clear CMOS

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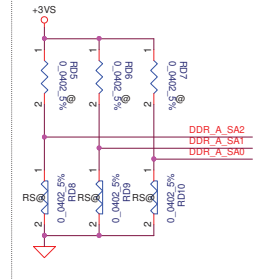
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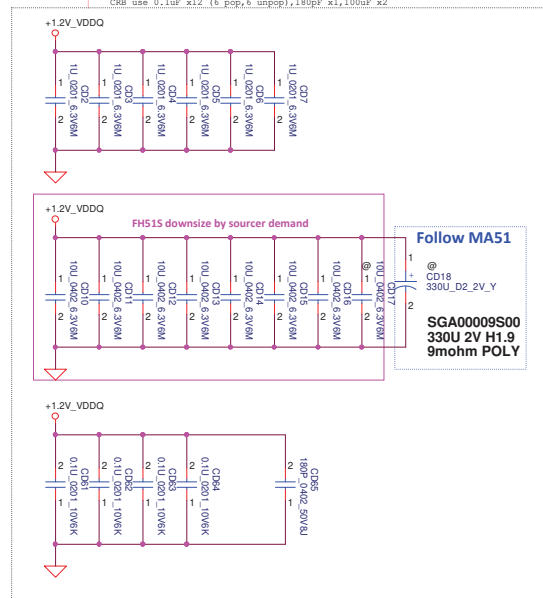
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Layout Note:  
Place near JDIMM1

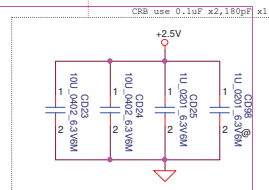
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

DDR4 support Even Parity check in DRAMs.

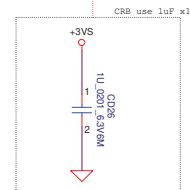


Layout Note:  
Place near JDIMM1.257,259

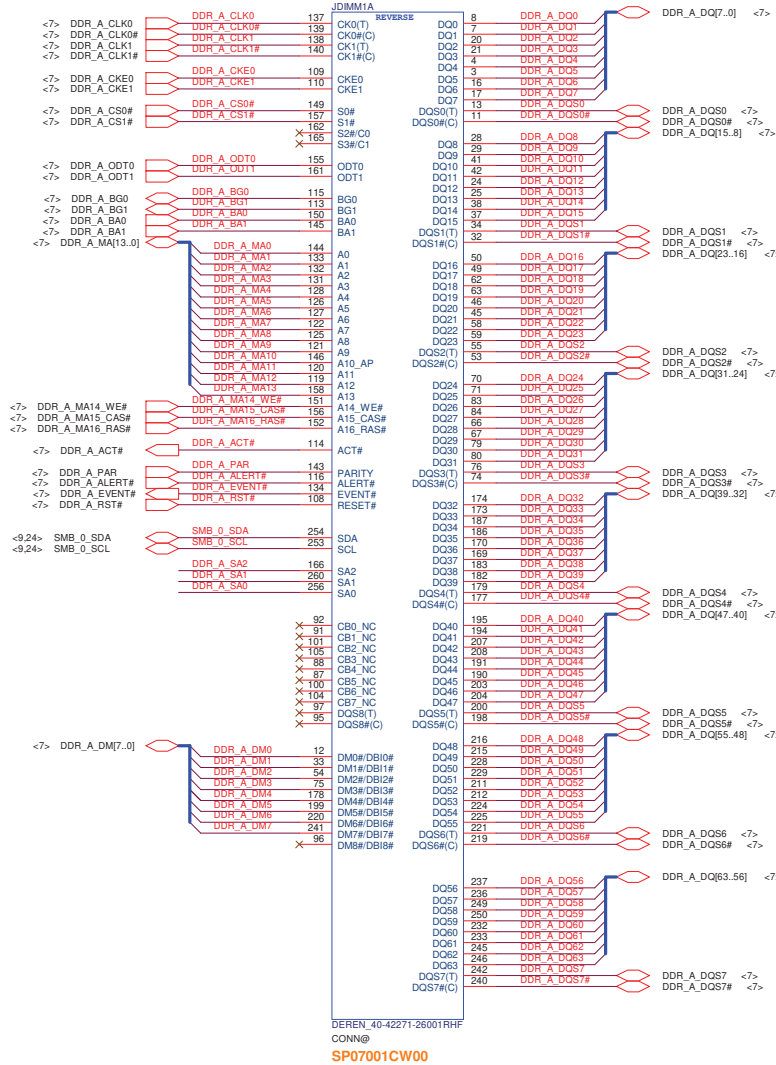
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FHS15 downsize by sourcer demand

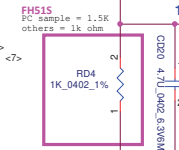


8/29



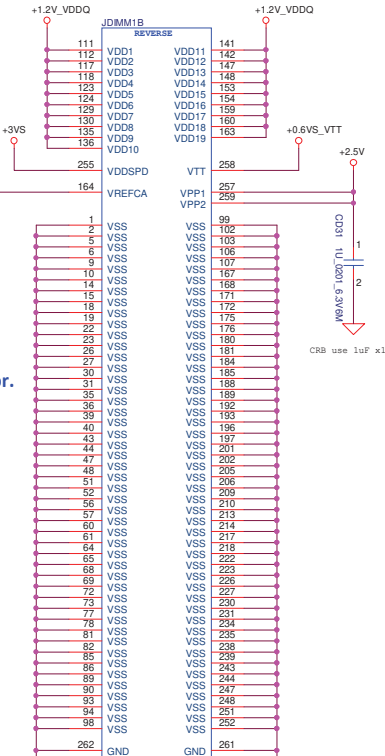
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CONN@  
SP07001CW00

Follow CRB design

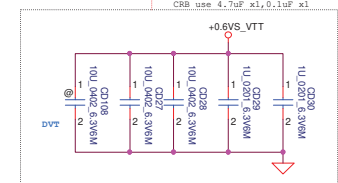


Place near to SO-DIMM connector.

Reverse Type  
2-3A to 1 DIMMs/channel



Layout Note:  
Place near JDIMM1.258



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2-3A to 1 DIMMs/channel

[illegible]

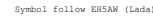
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

Figure 10 consists of three schematic diagrams labeled (a), (b), and (c), each showing a power supply configuration for the H515 device. Each diagram has a +1.2V\_VDDQ input at the top and a ground symbol at the bottom.

- (a) 12V\_VDDQ:** This diagram shows a series of capacitors connected to the +1.2V\_VDDQ input. From left to right, the capacitors are: CD71 (100 0201 6.3V6M), CD70 (100 0201 6.3V6M), CD69 (100 0201 6.3V6M), CD68 (100 0201 6.3V6M), CD67 (100 0201 6.3V6M), CD66 (100 0201 6.3V6M), and CD65 (100 0201 6.3V6M). The capacitors are connected in a chain, with the output of one capacitor connected to the input of the next.
- (b) H515 downsized by source demand:** This diagram shows a series of capacitors connected to the +1.2V\_VDDQ input. From left to right, the capacitors are: CD104 (100 0201 6.3V6M), CD103 (100 0201 6.3V6M), CD99 (100 0201 6.3V6M), CD98 (100 0201 6.3V6M), CD97 (100 0201 6.3V6M), CD96 (100 0201 6.3V6M), and CD95 (100 0201 6.3V6M). The capacitors are connected in a chain, with the output of one capacitor connected to the input of the next.
- (c) 1.2V\_VDDQ:** This diagram shows a series of capacitors connected to the +1.2V\_VDDQ input. From left to right, the capacitors are: CD65 (100 0201 6.3V6M), CD66 (100 0201 6.3V6M), CD67 (100 0201 6.3V6M), CD68 (100 0201 6.3V6M), CD69 (100 0201 6.3V6M), CD70 (100 0201 6.3V6M), and CD71 (100 0201 6.3V6M). The capacitors are connected in a chain, with the output of one capacitor connected to the input of the next.

[illegible]

A circuit diagram showing a 3V DC voltage source (labeled +3VS) connected in series with a capacitor (labeled 1u\_0201\_6.3V6M). The capacitor is represented by two parallel lines. The circuit is enclosed in a dashed rectangular box. The text "CRB use luF" is written at the top right of the diagram.

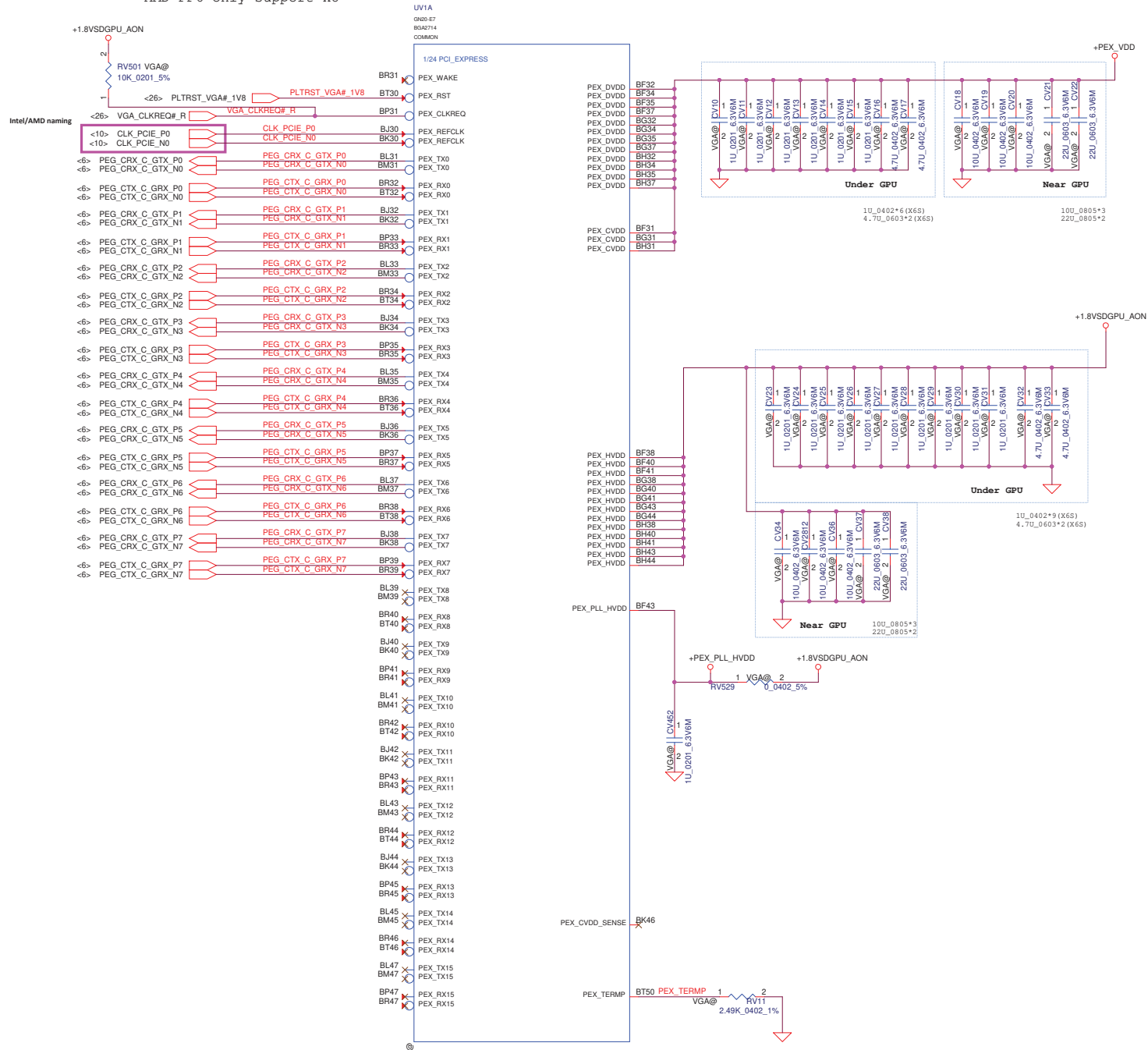


**Place near to SO-DIMM connector.**

The circuit diagram shows a 5-bit DAC implemented with an op-amp buffer and a resistor network. The op-amp is configured as a voltage follower, with its non-inverting input connected to the DAC output and its inverting input connected to ground. The DAC output is connected to the non-inverting input of the op-amp. The DAC output is also connected to a resistor network consisting of five resistors, each labeled  $1\mu 0.001\ 6.3\text{V}\text{M}$ . The resistors are connected in series between the DAC output and ground. The output of the DAC is labeled  $+0.6\text{V}_S\text{ VTT}$ . The DAC output is also connected to a resistor network consisting of five resistors, each labeled  $1\mu 0.001\ 6.3\text{V}\text{M}$ . The resistors are connected in series between the DAC output and ground. The output of the DAC is labeled  $+0.6\text{V}_S\text{ VTT}$ .

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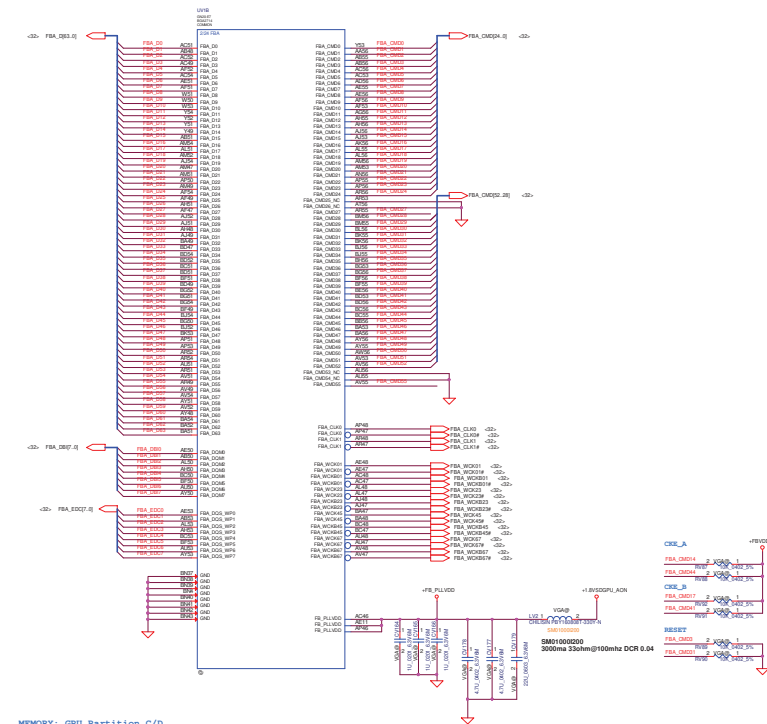
AMD FP6 only support x8



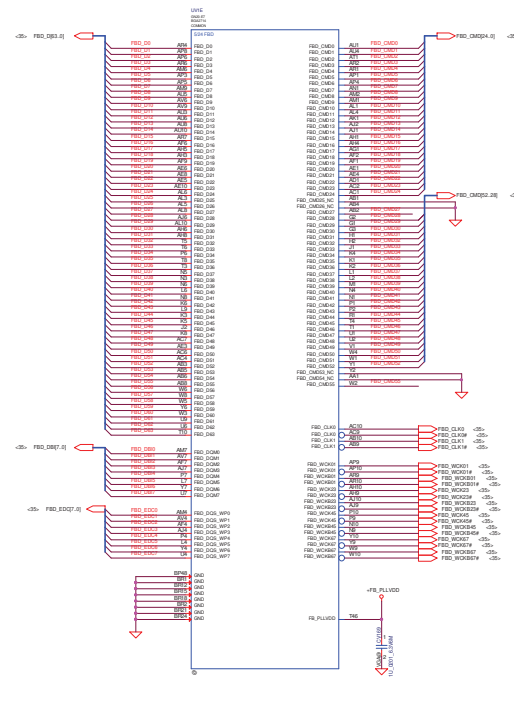
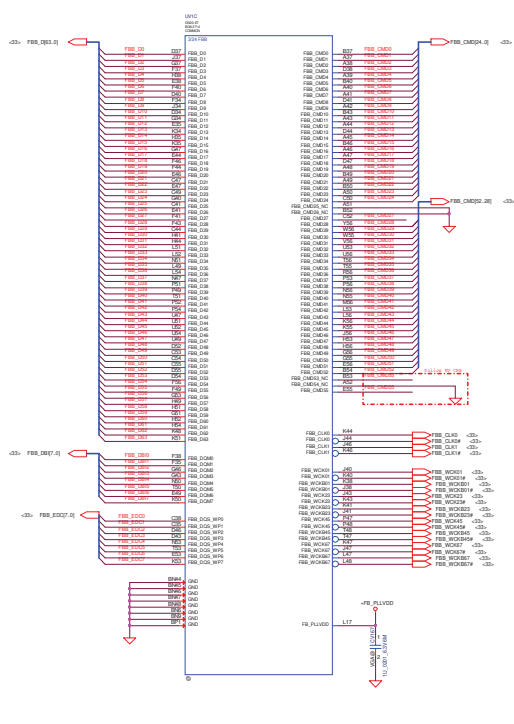
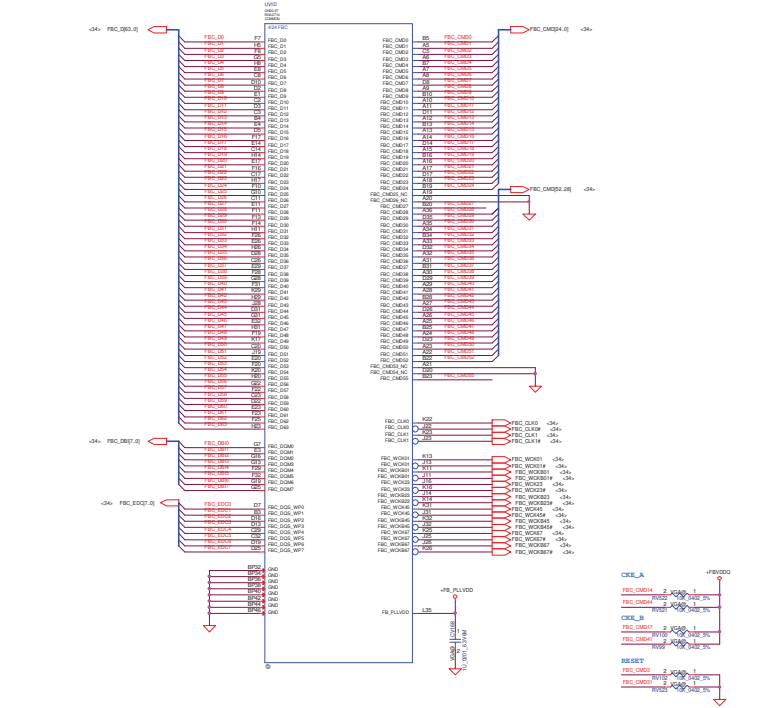
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Nvidia GN20-E5-A1  
E5QS@  
SA0000DUL00  
S IC GN20-E5-A1 FCBGA 2714 GPU S
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Nvidia GN20-E7-A1  
E7QS@  
SA0000DUM00  
S IC GN20-E7-A1 FCBGA 2714 GPU S
- UV1  
Nvidia GN20-E3-A1  
E3MP@  
SA0000E1930  
S IC GN20-E3-A1 FCBGA 2714 GPU ABO
- UV1  
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- UV1  
Nvidia GN20-E7-A1  
E7MP@  
SA0000DUM20  
S IC GN20-E7-A1 BGA 2714 GPU ABO!

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MEMORY: GPU Partition C/D

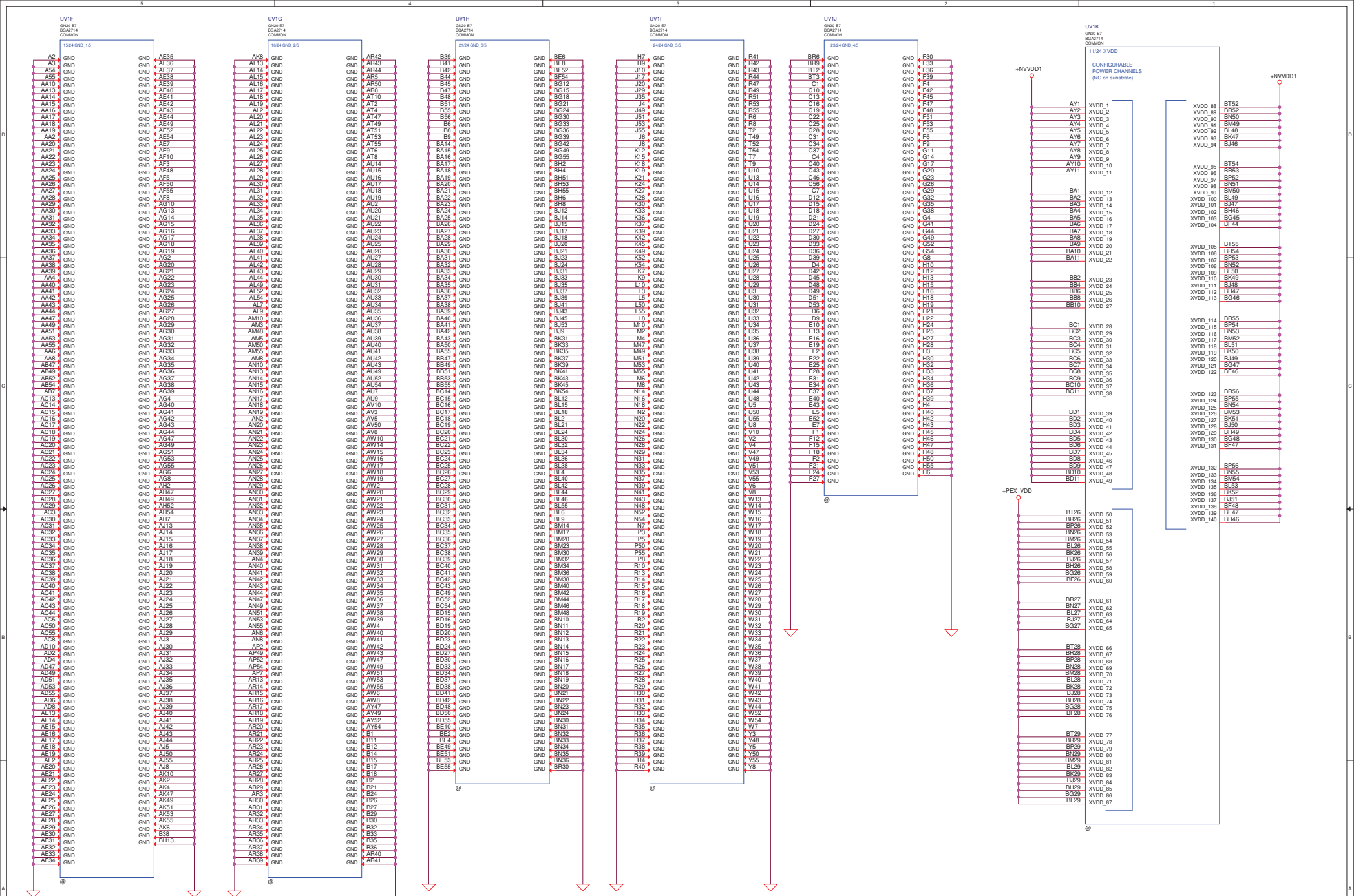












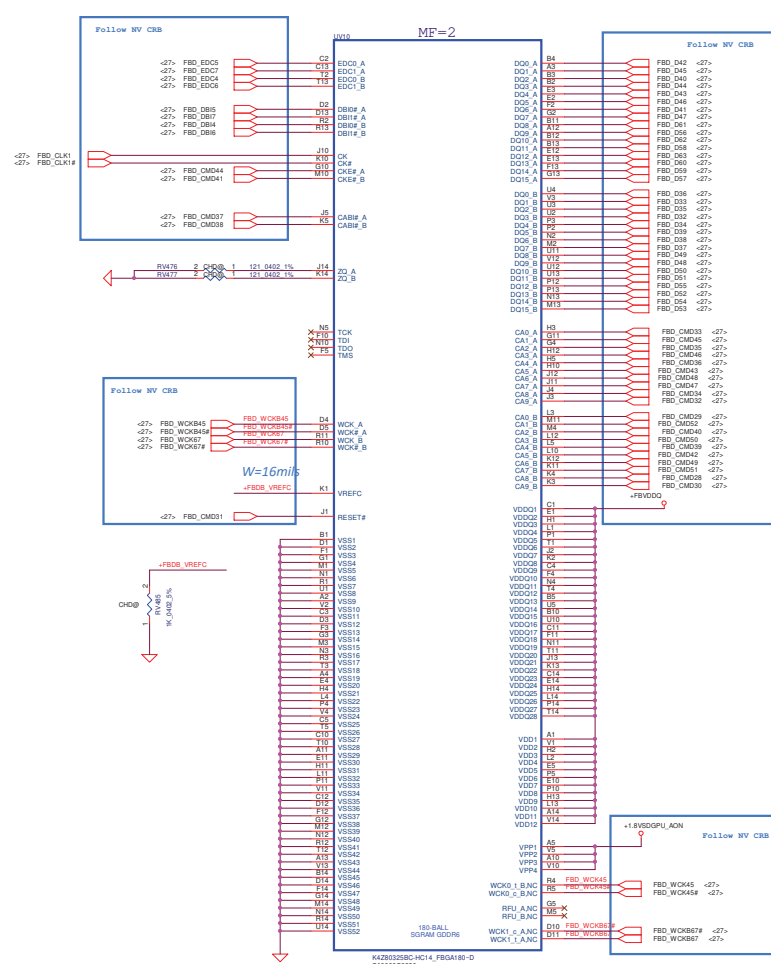








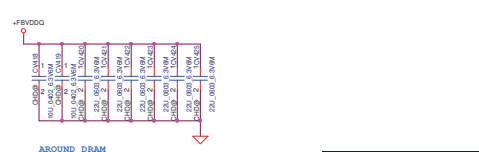
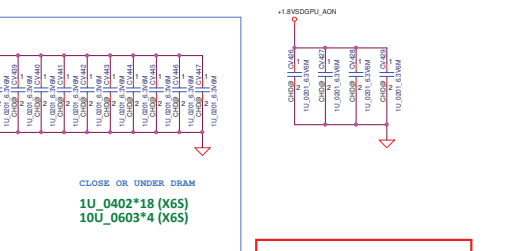


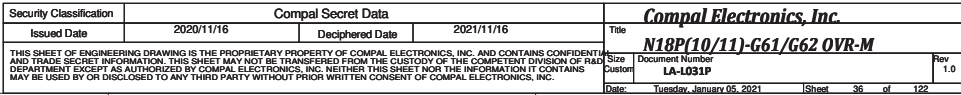


GB48-256		GPU FB3 Channel 0 (Data Bits [3:1]=0)	GB48-256	GPU FB3 Channel 1 (Data Bits [3:1]=32)
		[Bytes 4.1,2,3]		[Bytes 4.5,6,7]
FBx_CND14	Bytes 0:1, CA7 Bytes 2:1, CA7.B	FBx_CND10	Bytes 4:5, CA6 Bytes 6:7, CA7.A	
FBx_CND15	Bytes 0:1, CA8.A Bytes 2:1, CA8.B	FBx_CND11	Bytes 4:5, CA7.A Bytes 6:7, CA7.B	
FBx_CND32	Bytes 0:1, CA3.A Bytes 2:1, -----	FBx_CND13	Bytes 4:5, ----- Bytes 6:7, CA3.B	
GB48-256		GPU FB3 Channel 0 & 1		
FBx_CND34		DEBU0 <sup>1</sup>		
FBx_CND35		DEBU1 <sup>1</sup>		

Note:  
 1. GPU debug pins: not connected to DRAM.  
 2. Bytes 4.5 correspond to DRAM Channel A; Bytes 2.3 correspond to DRAM Channel B.  
 3. Bytes 4.6 correspond to DRAM Channel A; Bytes 6.7 correspond to DRAM Channel B.

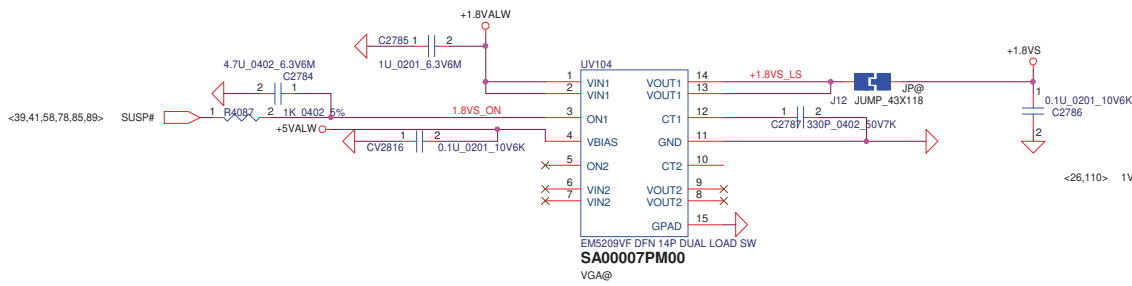
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.



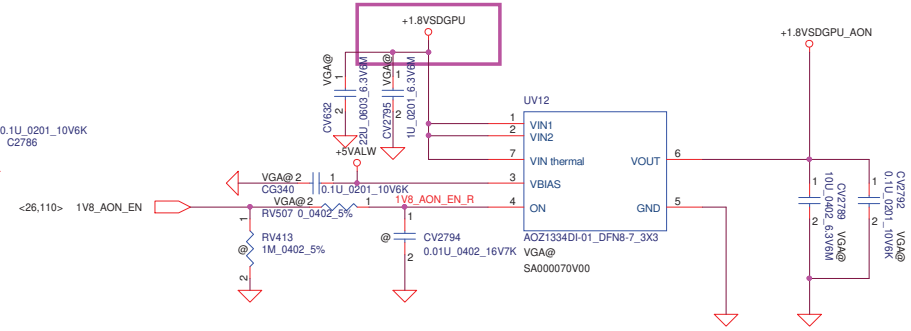




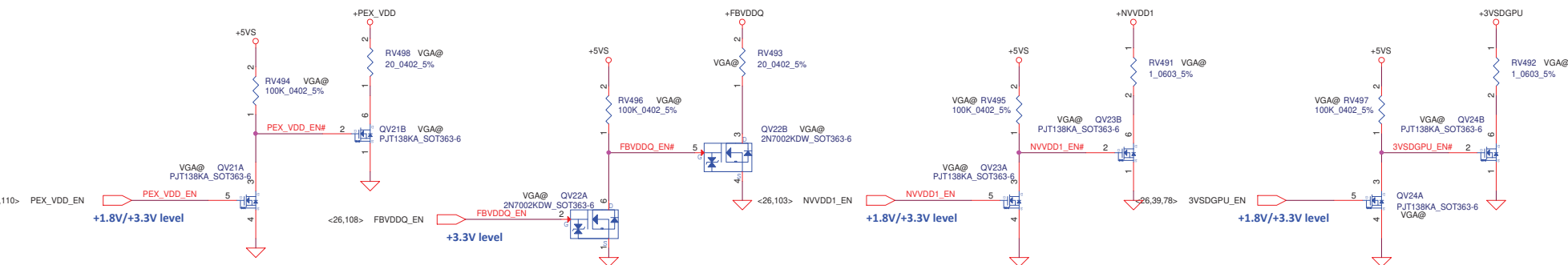
**/+1.8VS**



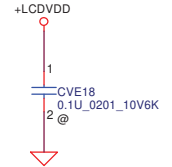
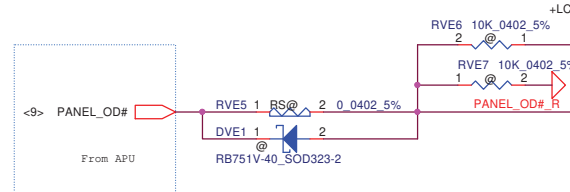
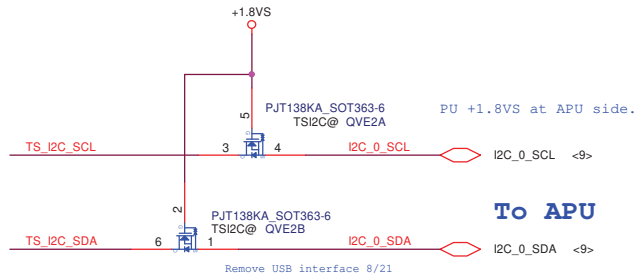
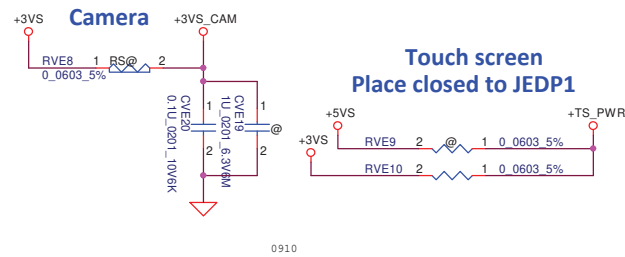
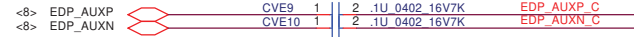
Intel/AMD naming



**For Power down sequence**



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TS\_I2C\_INT#

TS12C@

QVE1

2N7002KW 1N SOT323-3 -D SB000009Q80

3V5

RVE11

10K\_0402\_5%

TS2C@

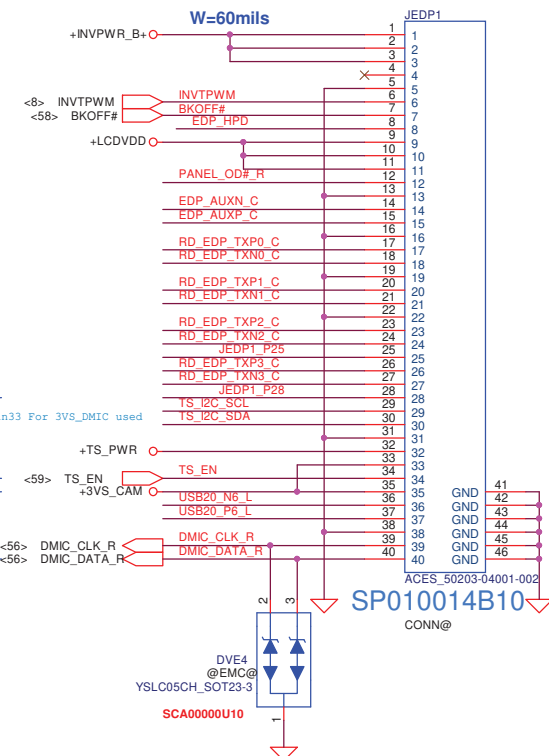
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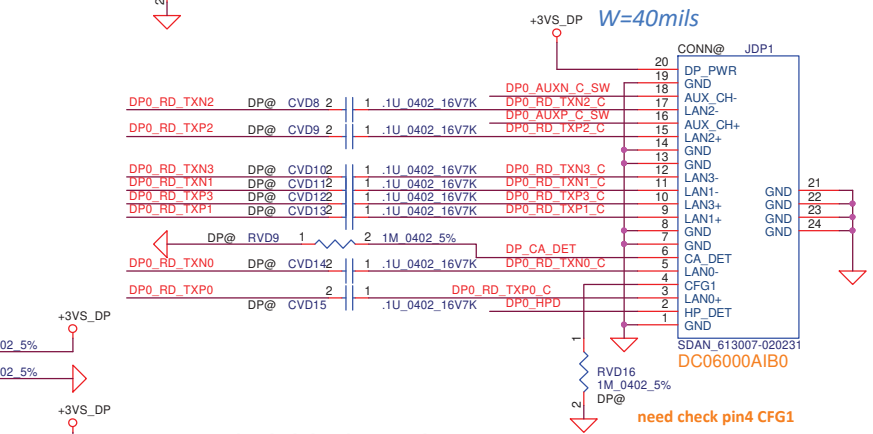
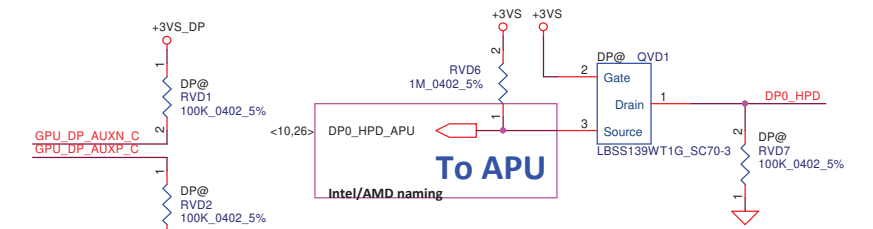
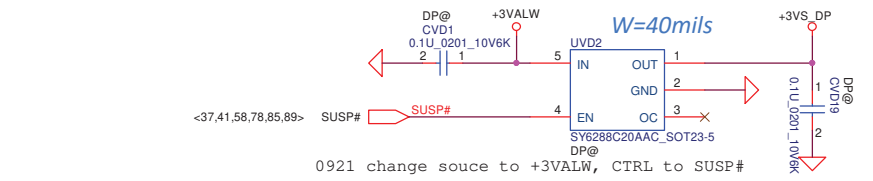
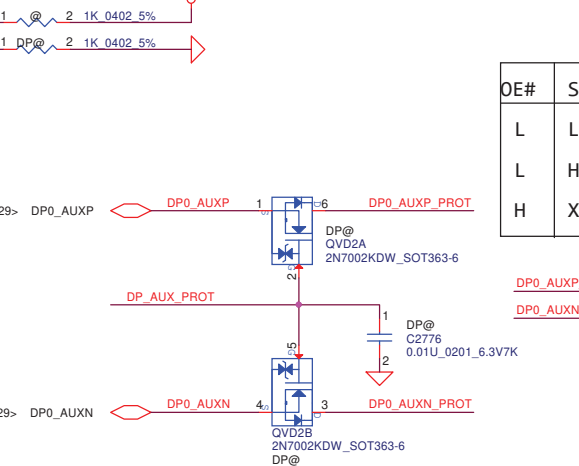
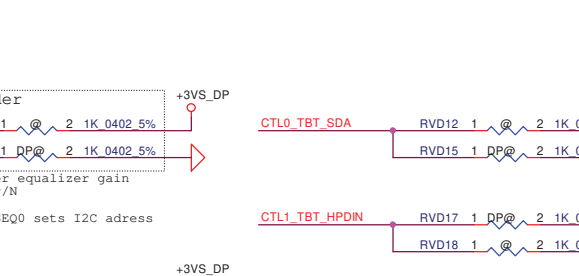
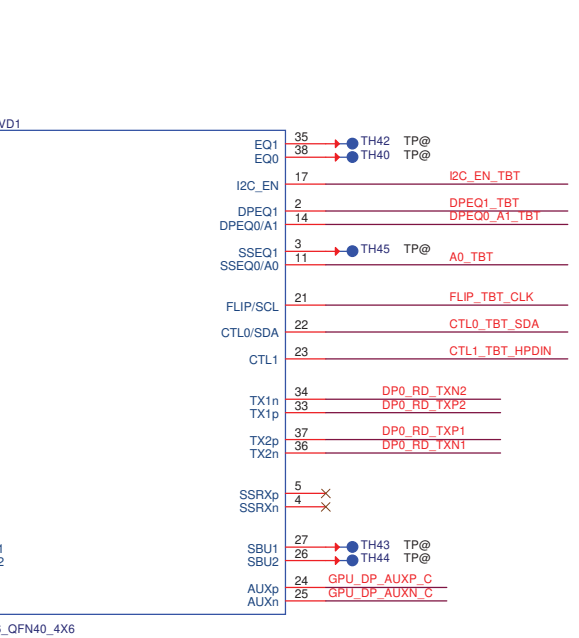
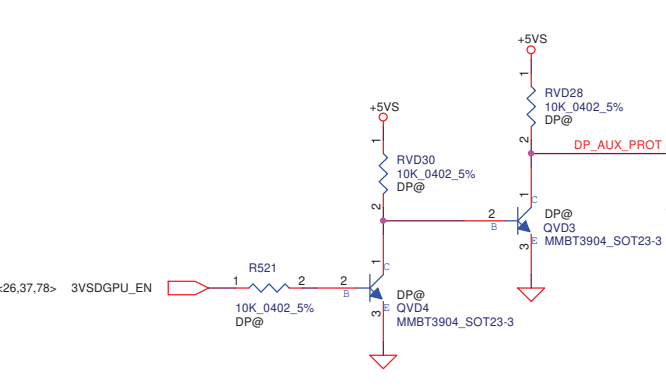
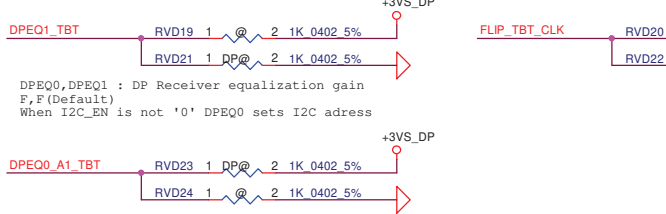
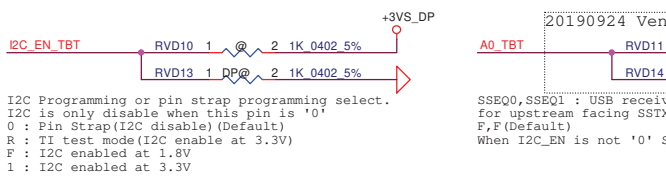
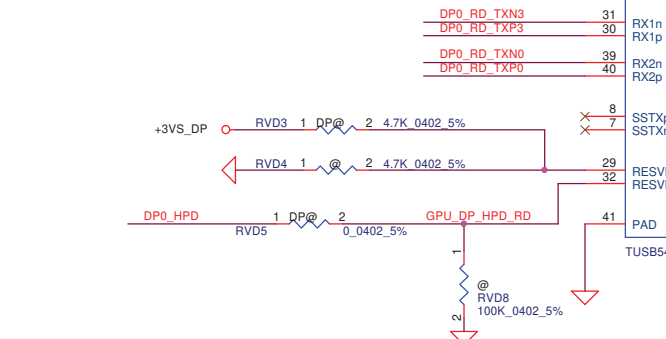
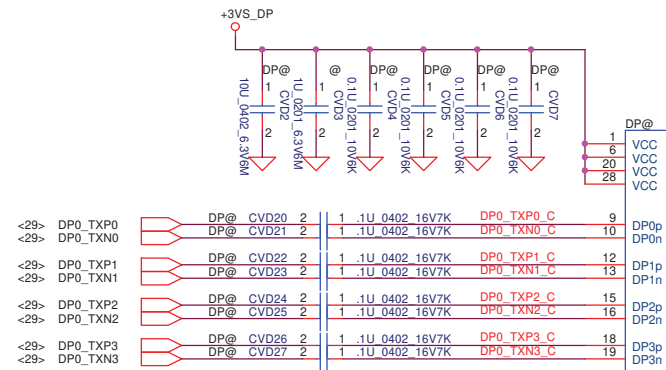
3V5

PU at APU side.

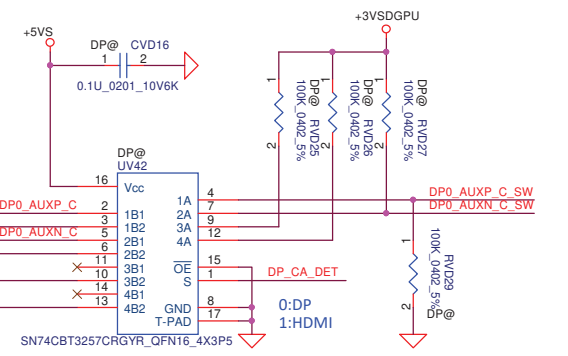
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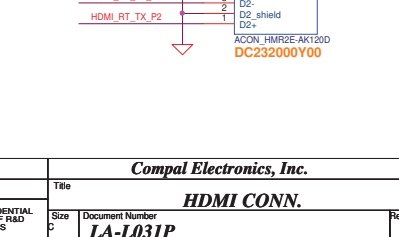
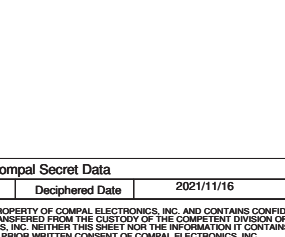
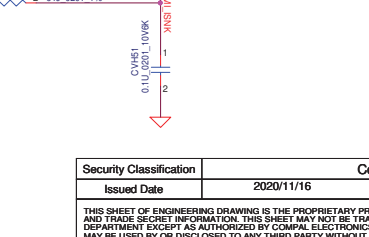
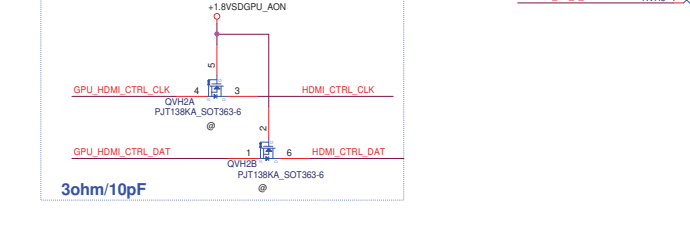
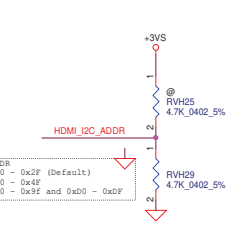
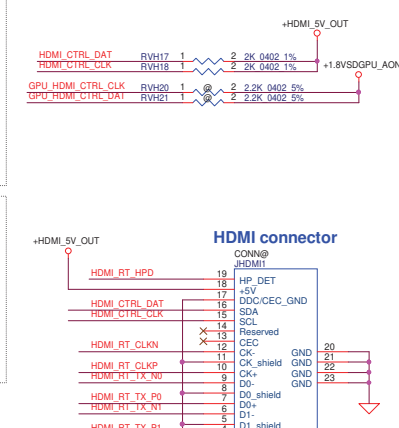
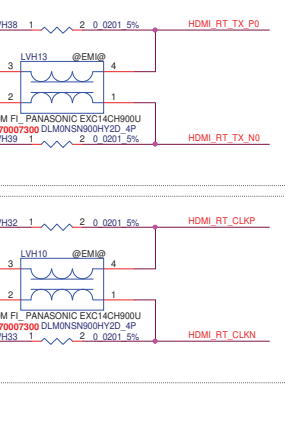
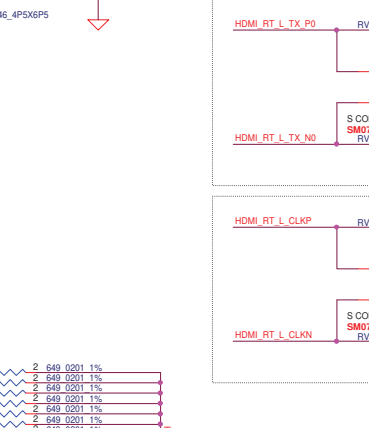
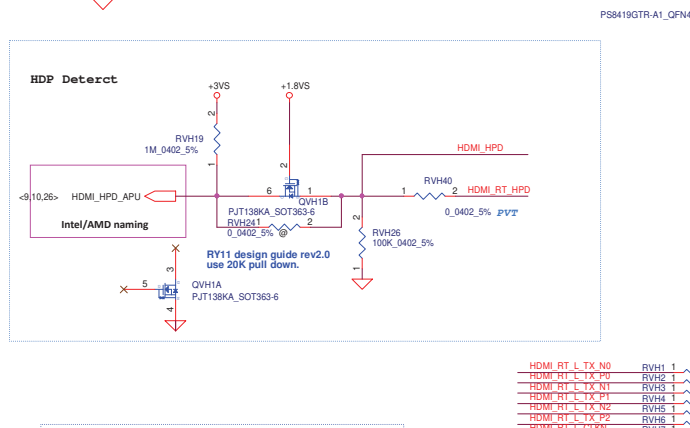
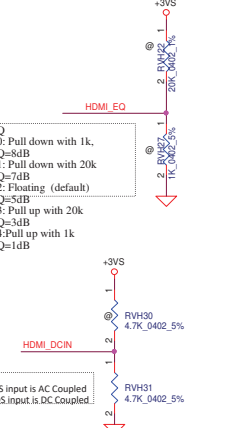
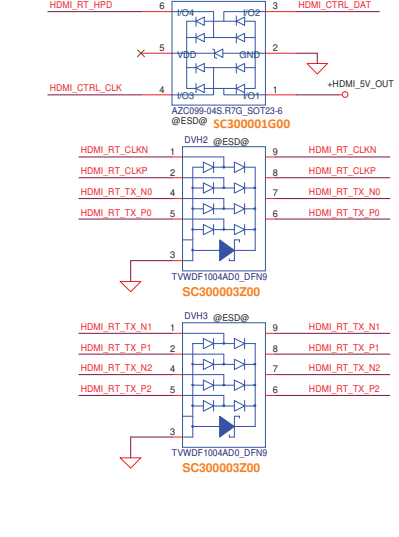
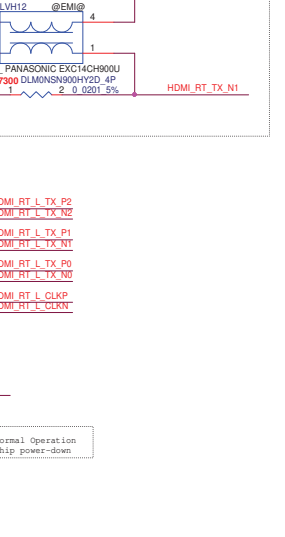
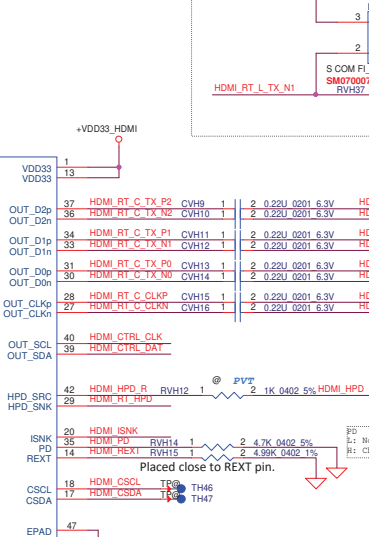
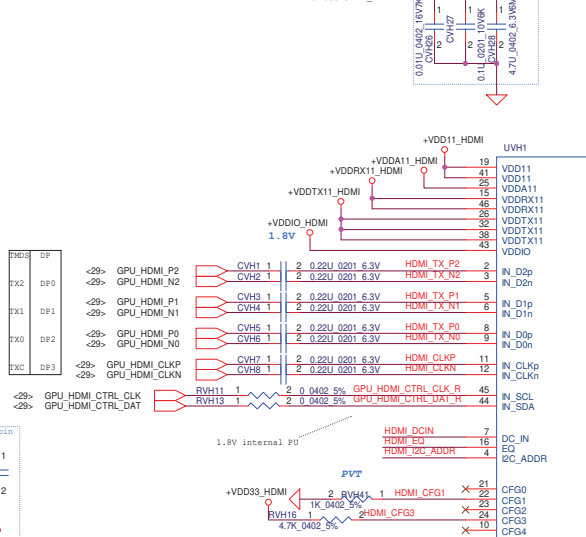
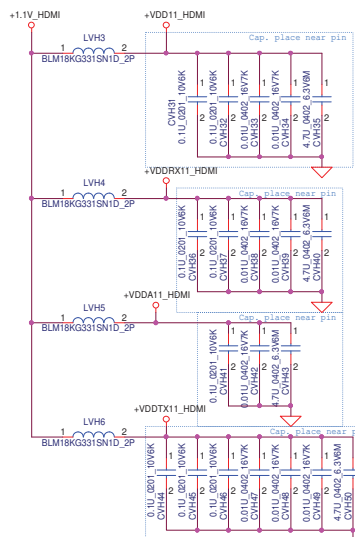
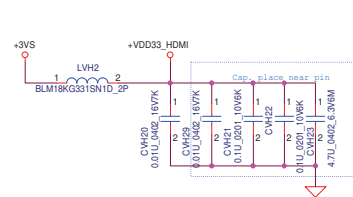
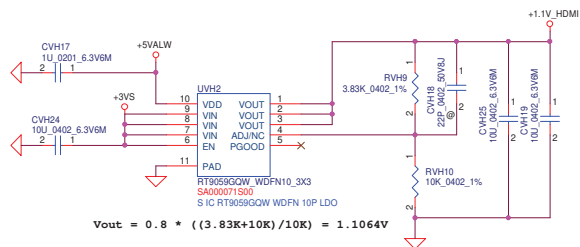


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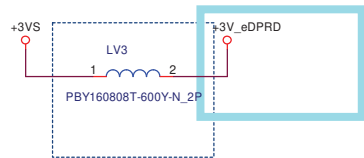


OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC



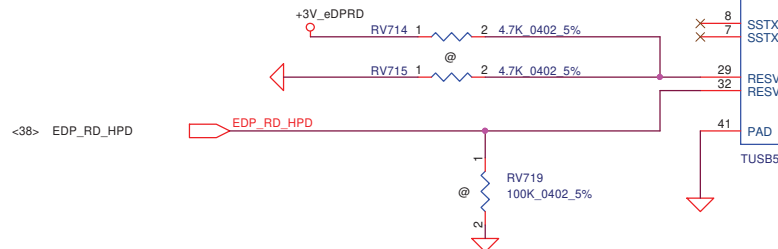
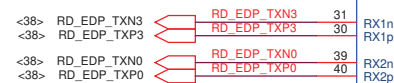
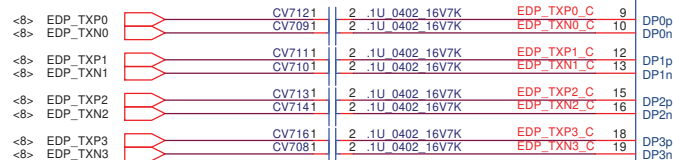
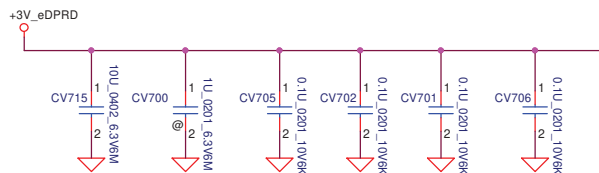
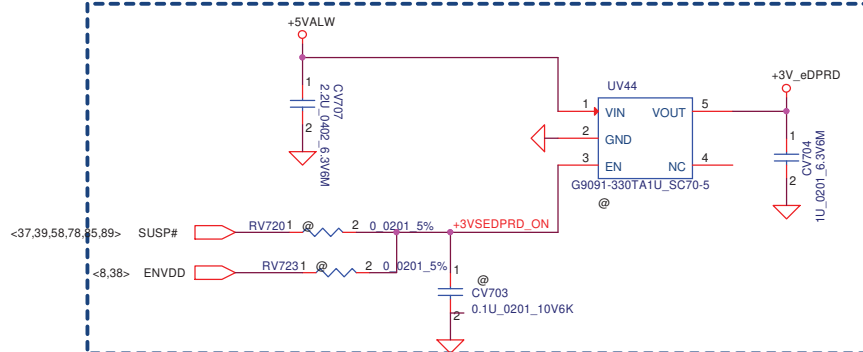


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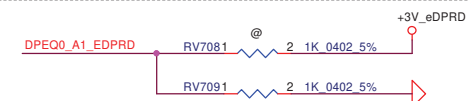


1012 check Ti if need

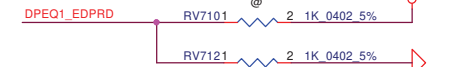
Reserve for 3V power supply



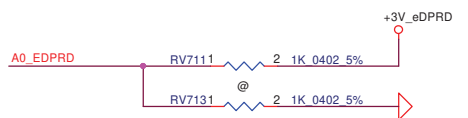
I2C Programming or pin strap programming select.  
I2C is only disable when this pin is '0'  
0 : Pin Strap(I2C disable)(Default)  
R : TI test mode(I2C enable at 3.3V)  
F : I2C enabled at 1.8V  
1 : I2C enabled at 3.3V



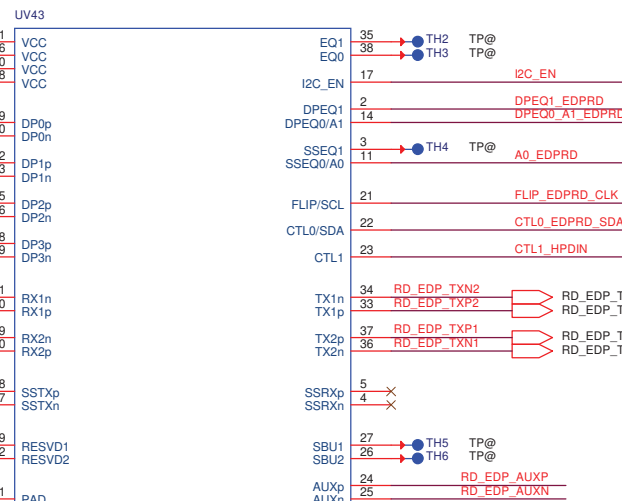
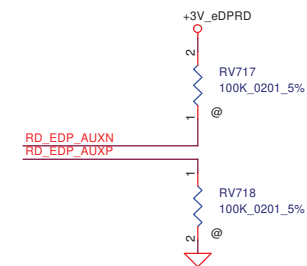
PVT change 0,0



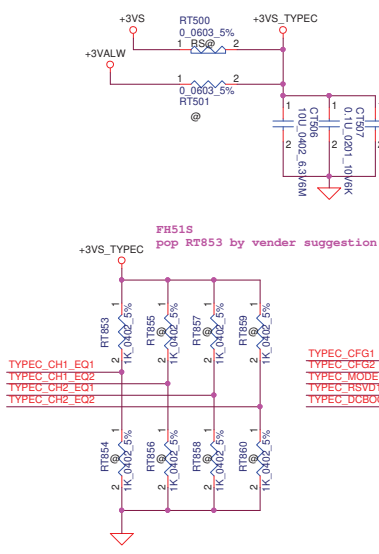
DPEQ0,DPEQ1 : DP Receiver equalization gain  
F,F(Default)  
When I2C\_EN is not '0' DPEQ0 sets I2C address



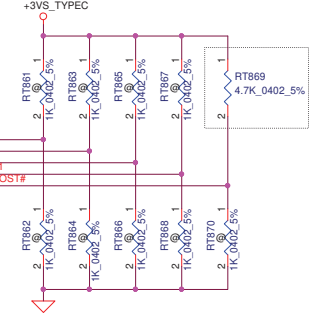
SSEQ0,SSEQ1 : USB receiver equalizer gain  
for upstream facing SSTXP/N  
F,F(Default)  
When I2C\_EN is not '0' SSEQ0 sets I2C address



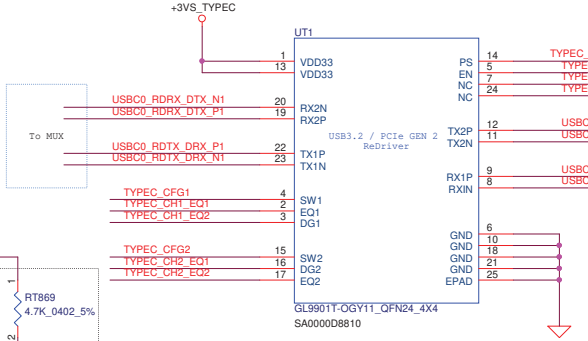
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TYPEC\_CH1\_EQ1  
TYPEC\_CH1\_EQ2  
TYPEC\_CH2\_EQ1  
TYPEC\_CH2\_EQ2

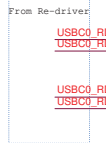
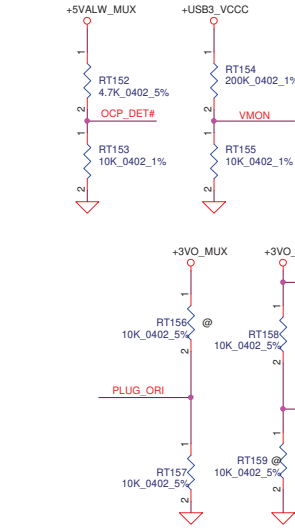
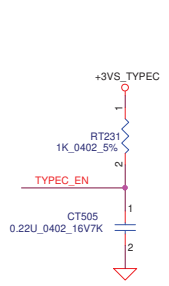
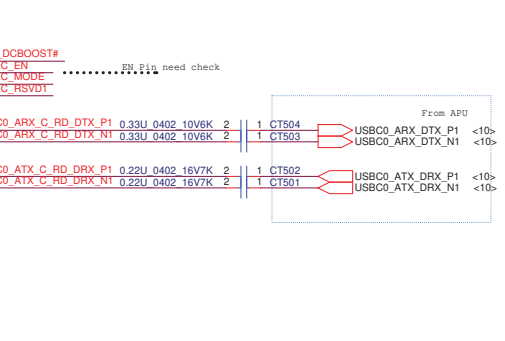


TYPEC\_CFG1  
TYPEC\_CFG2  
TYPEC\_MODE  
TYPEC\_RSVD1  
TYPEC\_DCBOOST#



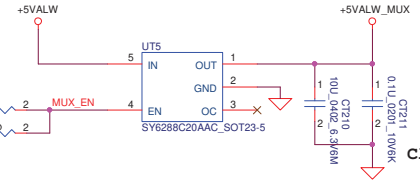
2	3	4	15	17	16	14
SW1	EQ1	DG1	SW2	EQ2	DG2	PS
F	F	F	F	F	F	H

substitute part:SA0000EAEO0

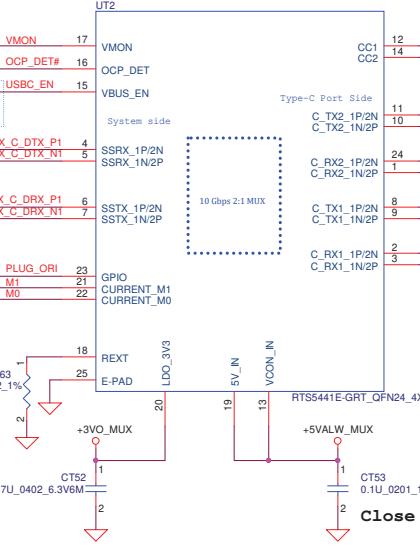


FB51S  
TX change to 0.22u  
(Vender suggestion)

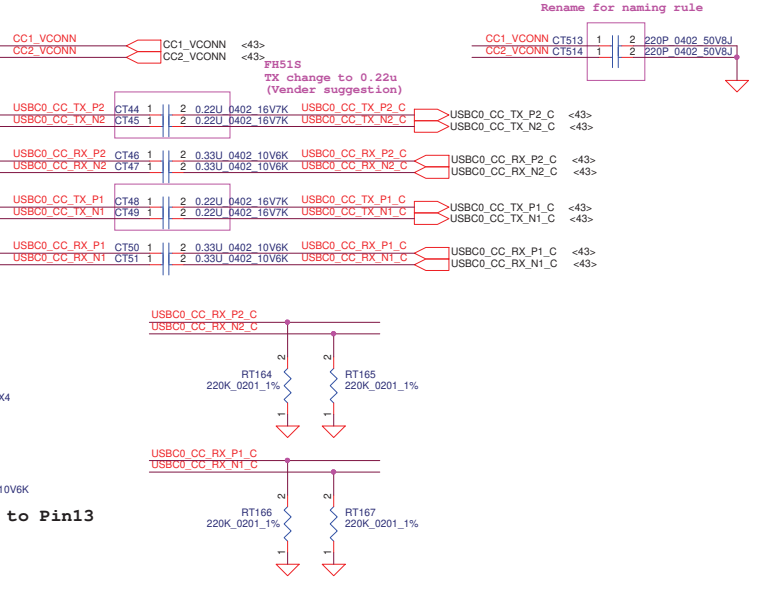
<43> OCP\_DET#  
<43> USB\_EN



Close to Pin19



Close to Pin13

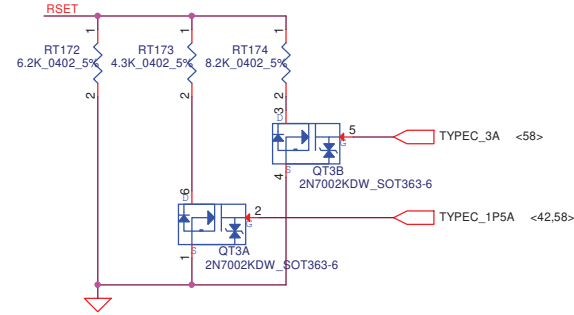
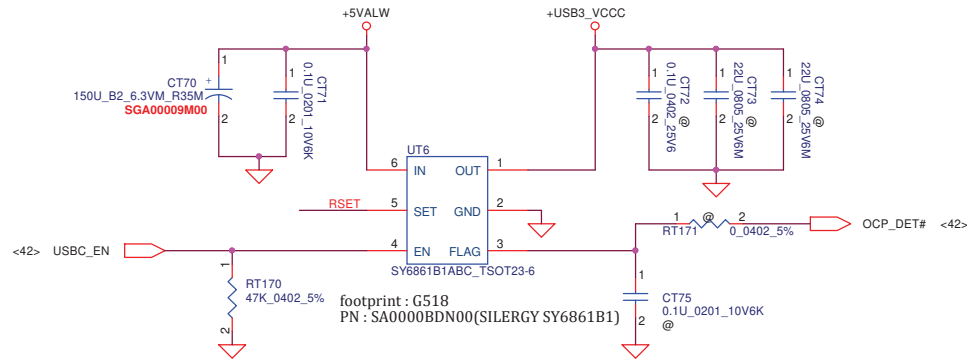


Rename for naming rule

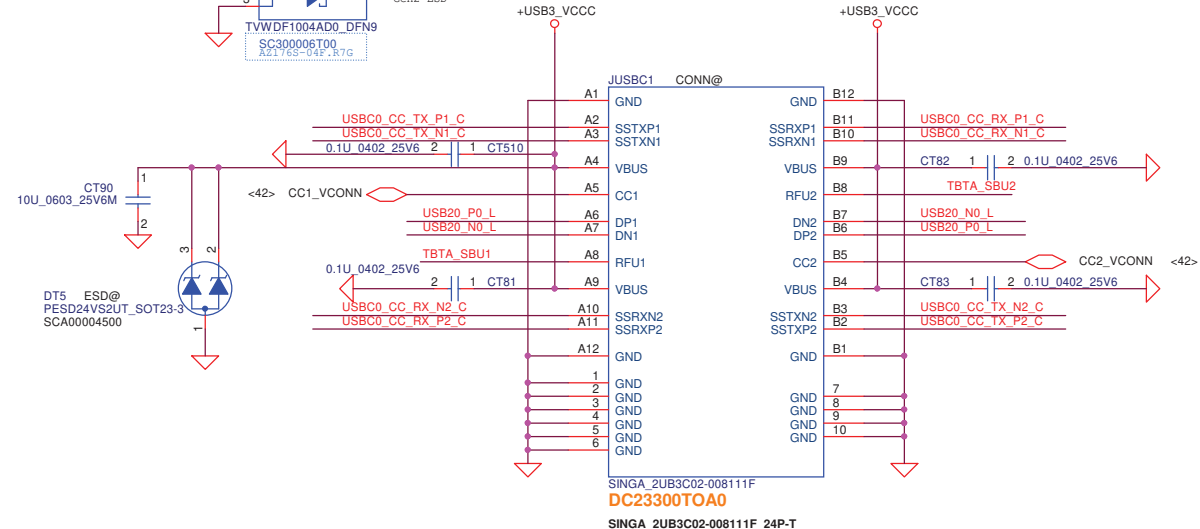
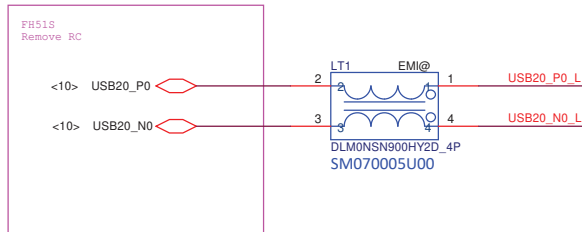
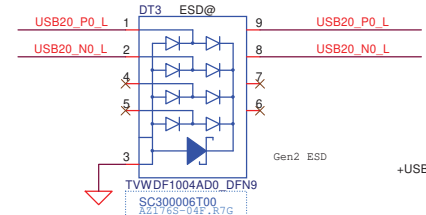
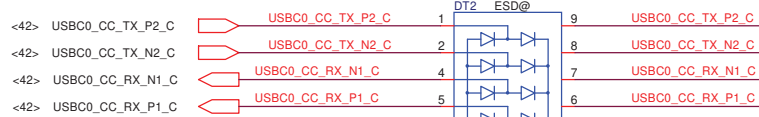
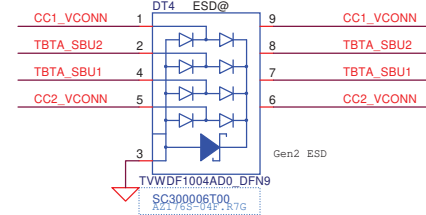
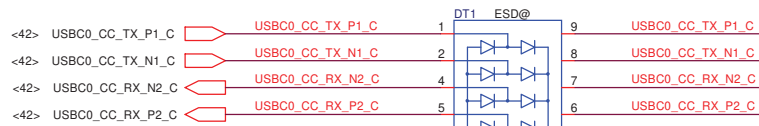
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

confirm realtek hand-shake



SILERGY SY6861B1 MOS Current Limit				
TYPEC_1P5A	TYPEC_3A	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



CC1\_VCONN & CC2\_VCONN need 20mil trace width.

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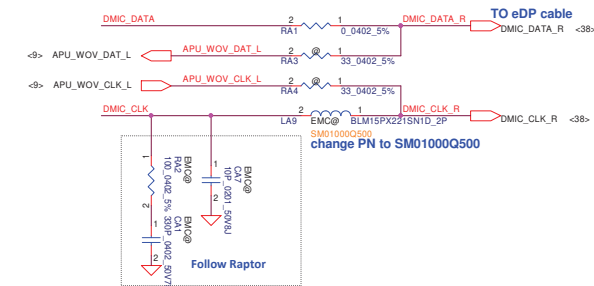
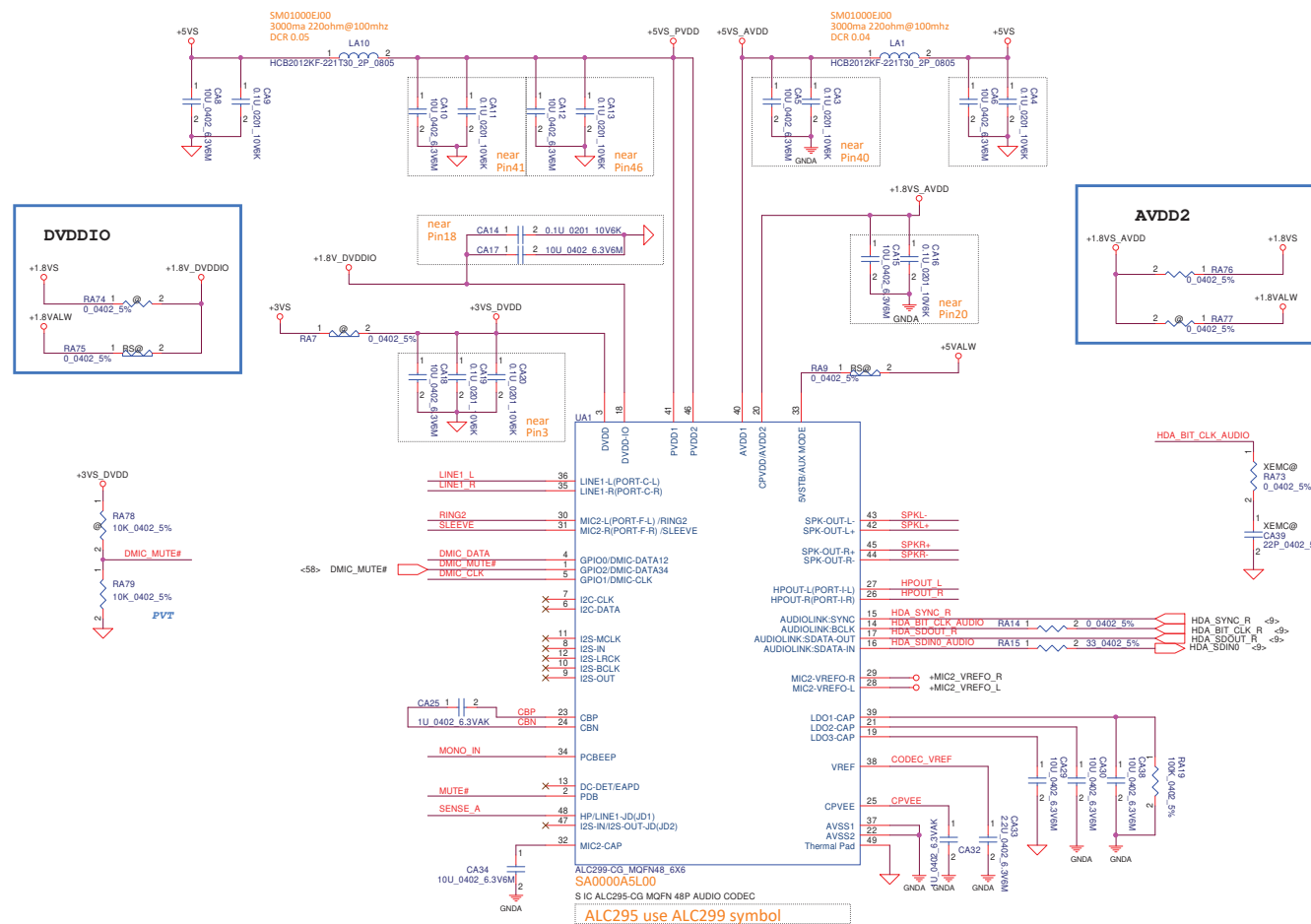
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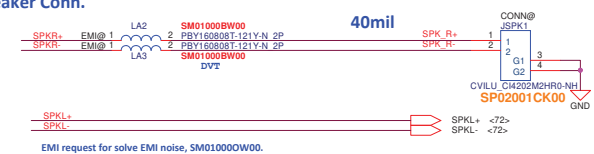


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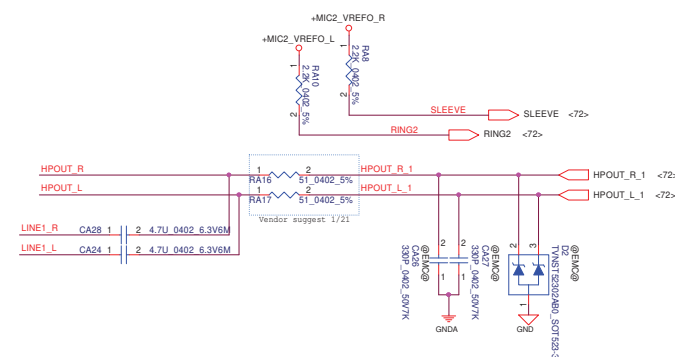
## HD Audio Codec



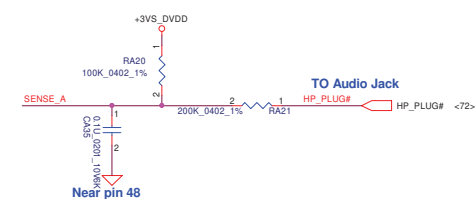
## Int. Speaker Conn.



## Headphone Out



## JACK Detect

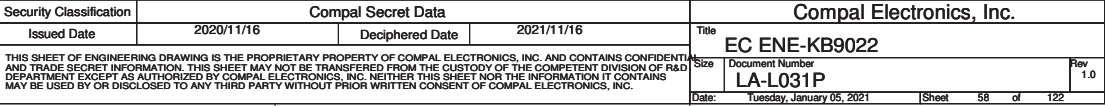


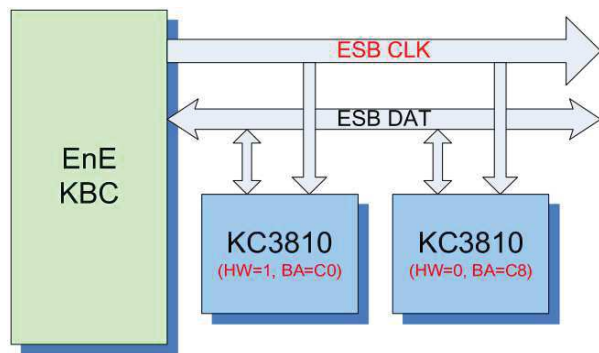
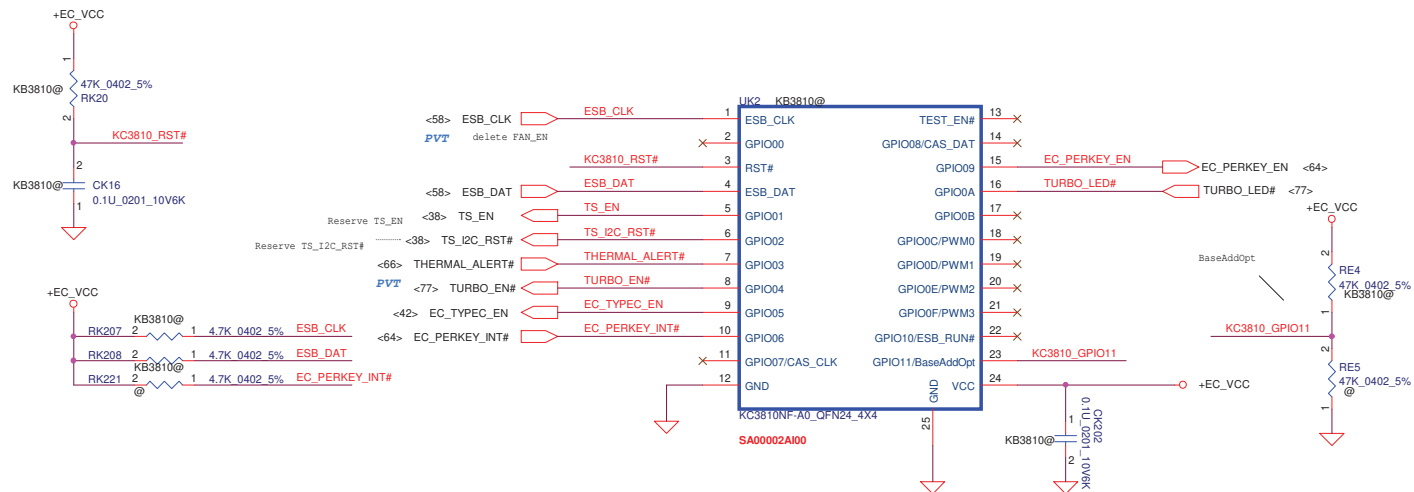
JD1	
HP-JD	LINE1-JD
200K	100K

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				Date:	January 09, 2021
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					Size	Document Number LA-L031P		Rev 1.0
					Date: Tuesday, January 05, 2021			Sheet 60 of 122



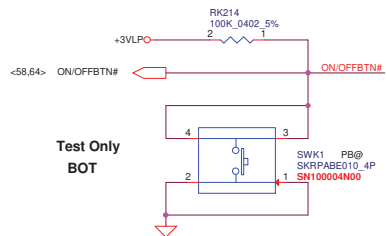
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					Size	Document Number LA-L031P		Rev 1.0			
					Date: Tuesday, January 05, 2021					Sheet	61 of 122

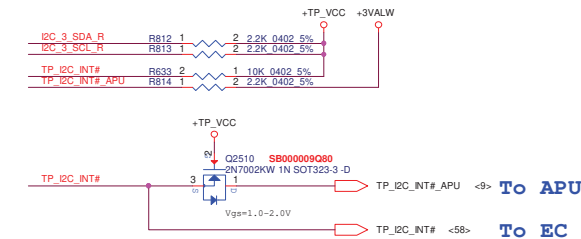
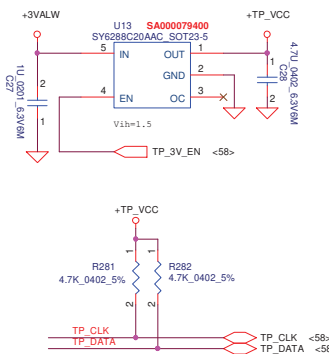
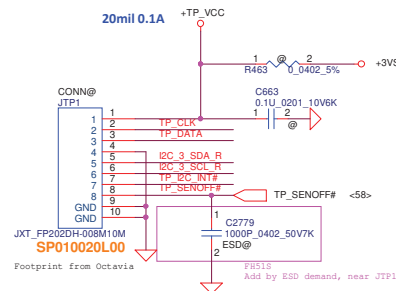
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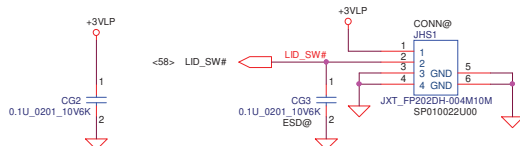
## ON/OFF BTN



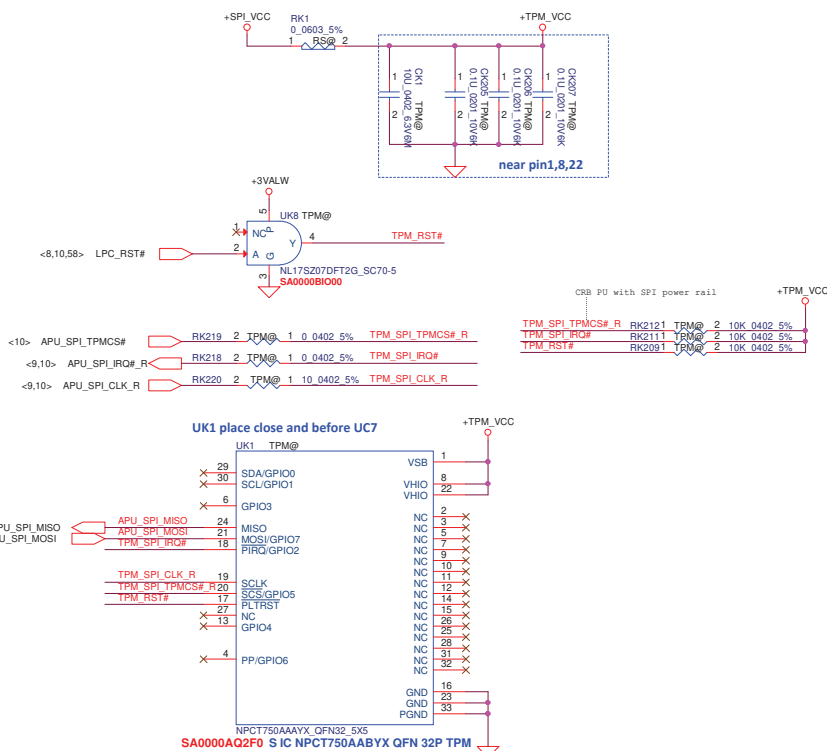
## TP/B Conn.



## Lid Switch (Hall Effect Switch)

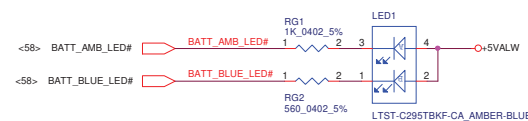


## TPM

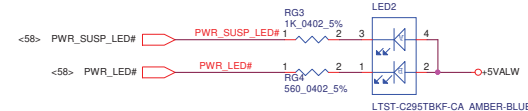


## LED

### Battery LED

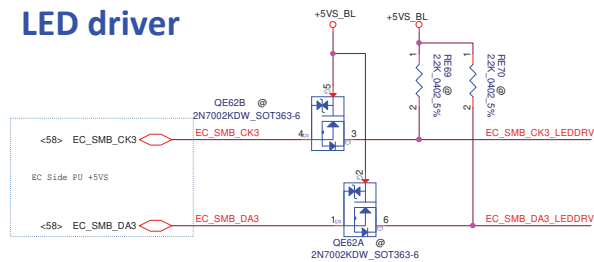


### Power LED

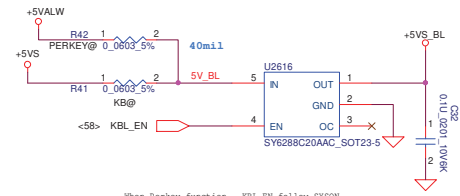


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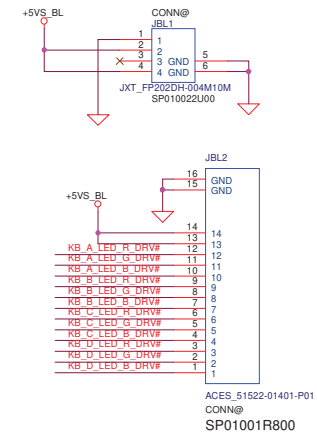
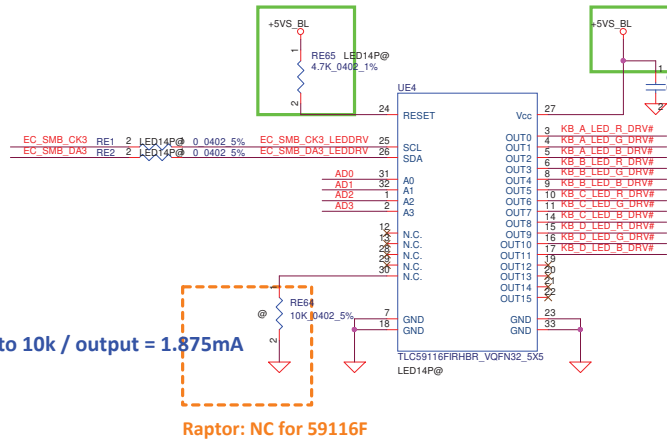
## LED driver



## KB BackLight

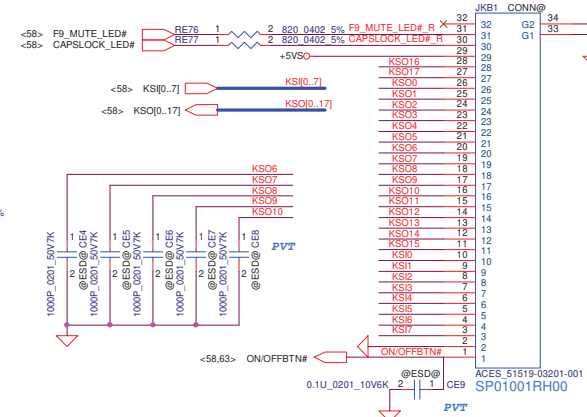
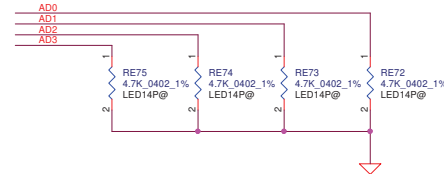
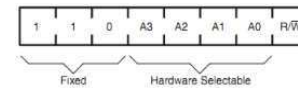


When Perkey function , KBL\_EN follow SYSON

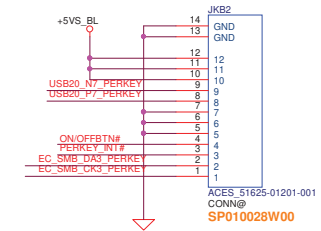
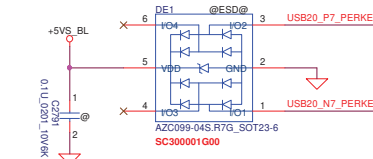
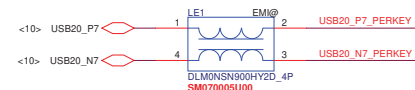
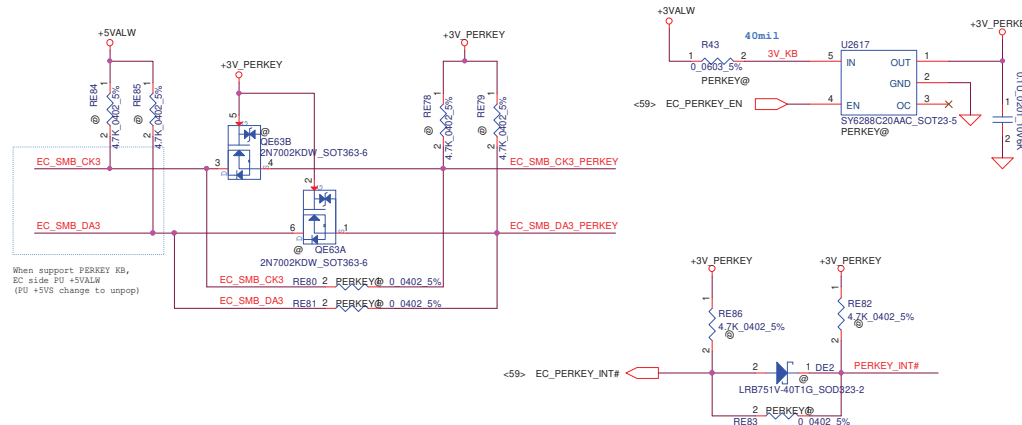
**KB Conn.**

set RE7 to 10k / output = 1.875mA

**Raptor: NC for 59116F**



### Per Key Conn.

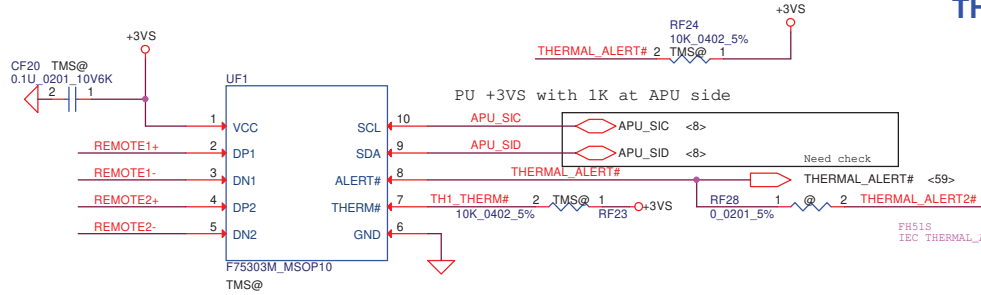
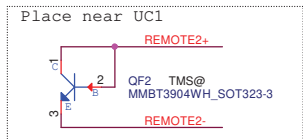
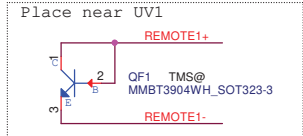
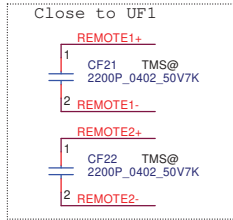


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Date:				Tuesday, January 05, 2021	Sheet	64 of 122

Reserve

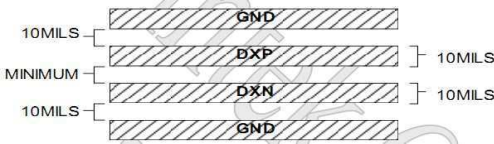
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				Date:	Tuesday, January 05, 2021	Sheet 65 of 122

## THERMAL SENSOR

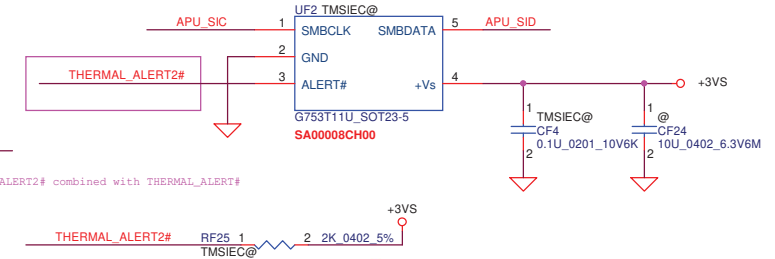


Part Number	SMBus Address
F75303M	1001_101xb

REMOTE1,2 (+/-) :  
Trace length: <8"



## THERMAL IEC



The G753 has the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G753	1	0	0	1	0	0	0

The G753 also responds to the SMBus Alert Response slave address (see the Alert Response Address section).

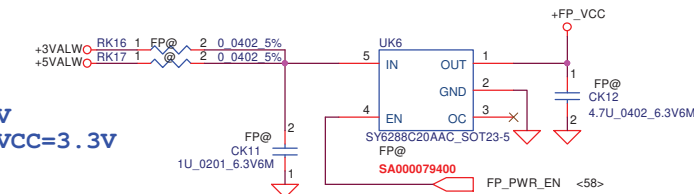
**ALERT# point hardware power-on setting**

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

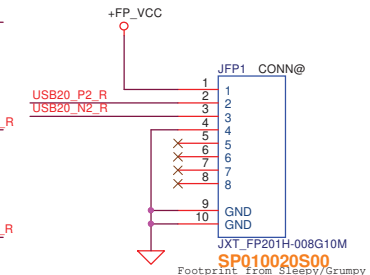
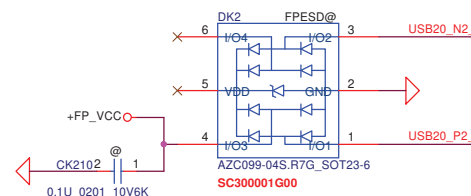
PULL-UP RESISTOR	TEMPERATURE (°C)
2kΩ	75
7.5kΩ	90
10.5kΩ	100
14kΩ	105
18.7kΩ	110

## Finger Print

Power Source Check  
EGIS ETU801 +FP\_VCC=5V  
ELAN SA464K-2200 +FP\_VCC=3.3V



PIN	SA464K-2200
1	+FP_VCC (3V)
2	D+
3	D-
4	GND
5	NC
6	NC
7	NC
8	NC



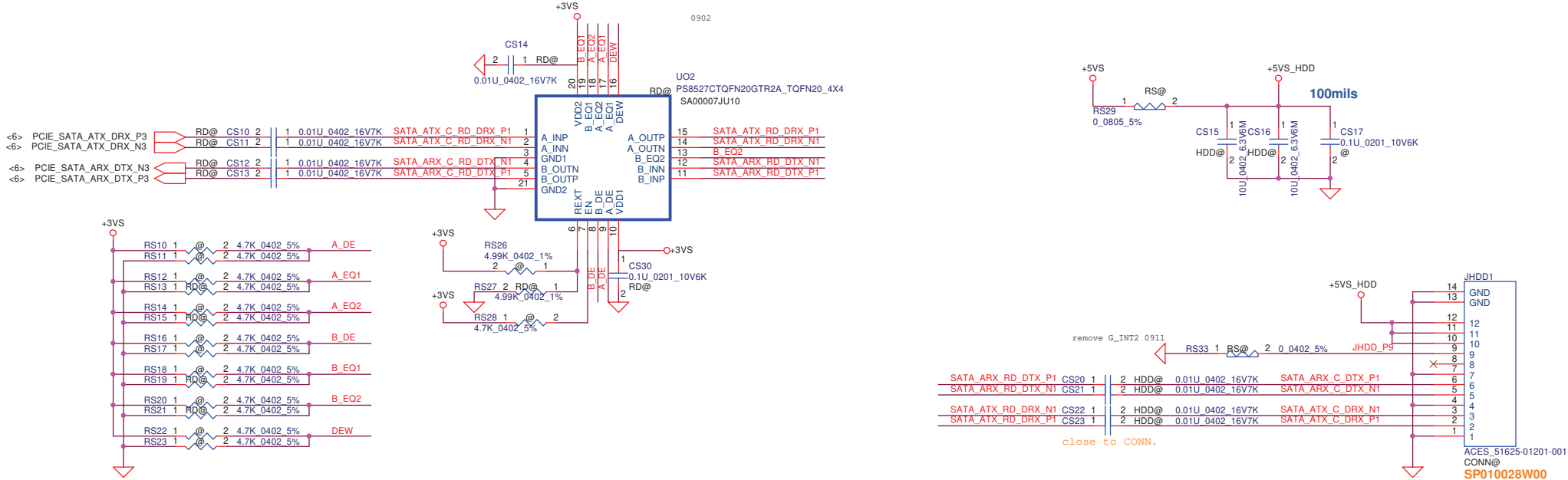
www.teknisi-indonesia.com

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				Size
				Document Number
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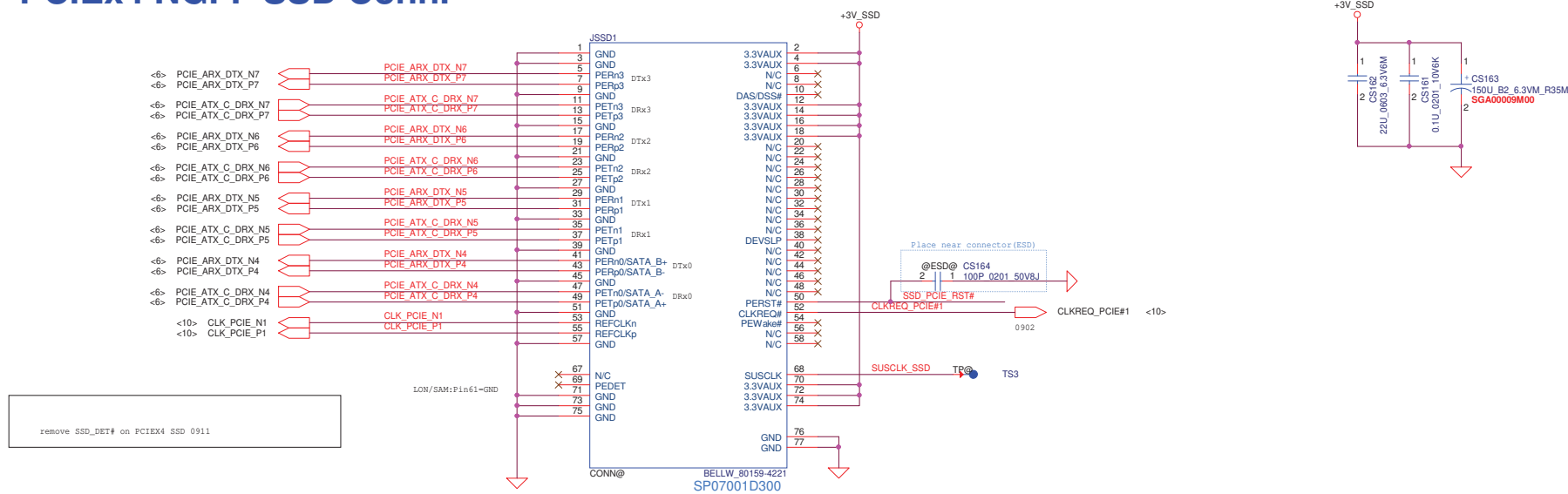
SATA Re-Driver



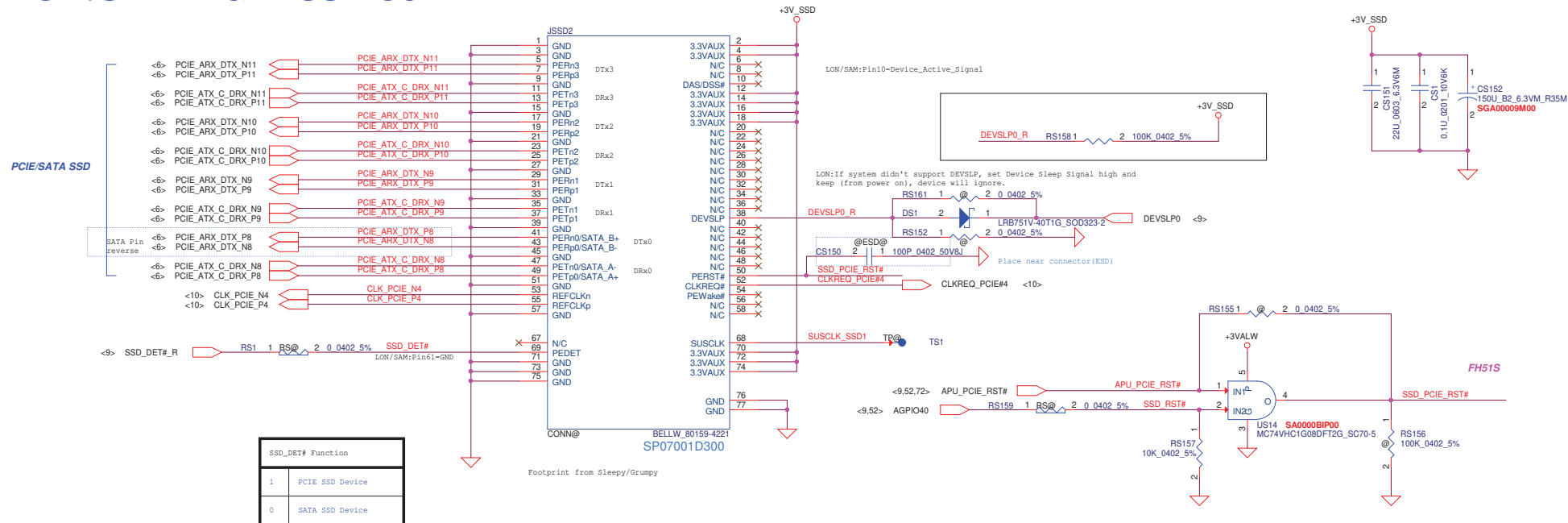
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						Size	Document Number			Rev	
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# PCIEx4 NGFF SSD Conn.



# PCIe/SATA NGFF SSD Conn.



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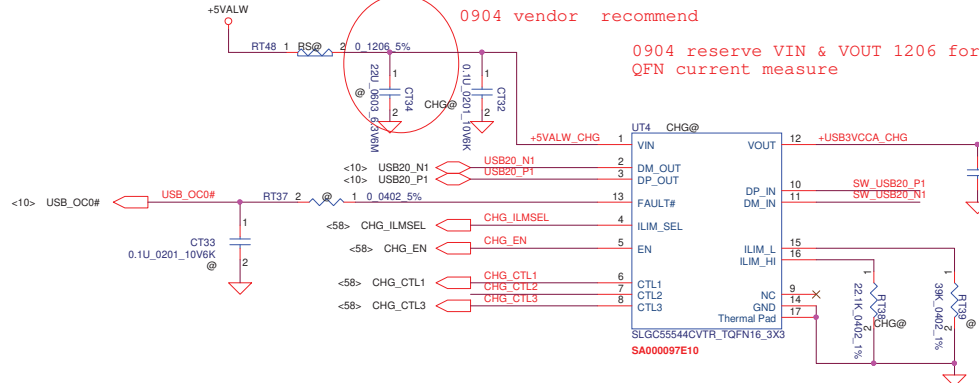
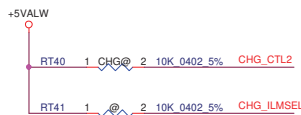
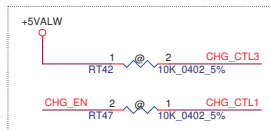
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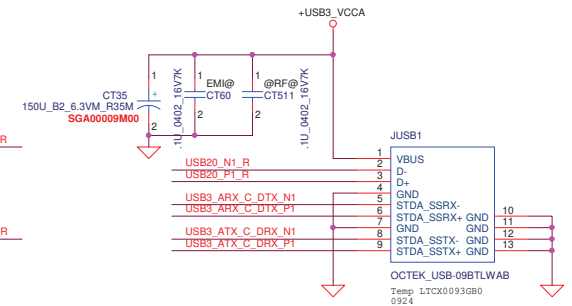
## USB Host Charger Truth Table

CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	SDP1	ILIM_H	Data Lines Connected
1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	CDP	ILIM_H	Data Lines Connected

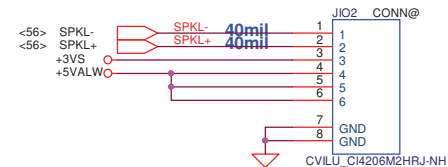
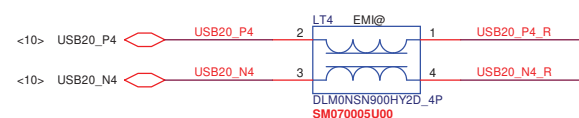
CHG_EN	CTL1
0	0
1	0
1	0
1	1



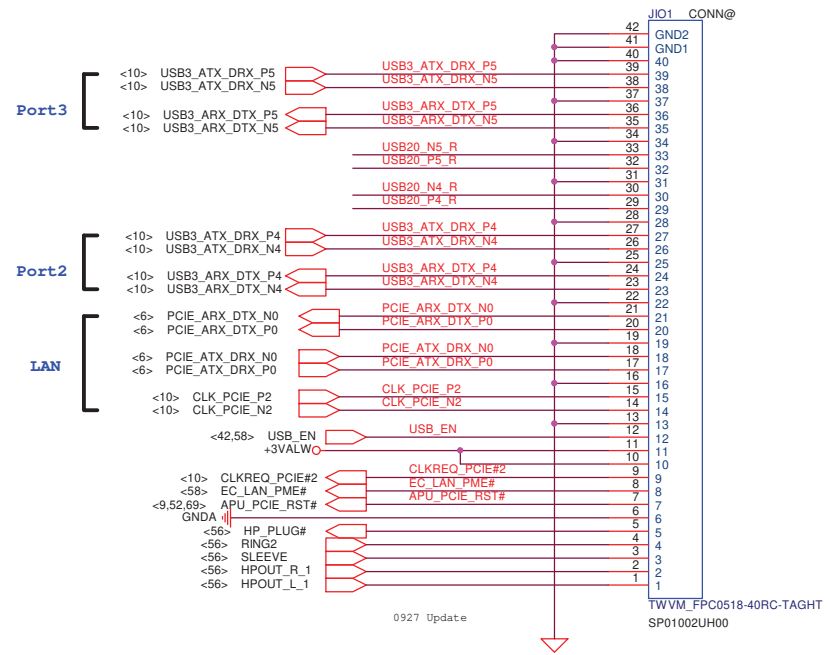
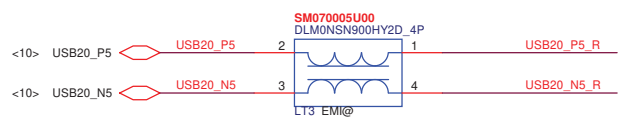
## USB3.0 Conn.



# USB3.0 (Port 2)



# USB3.0 (Port 3)



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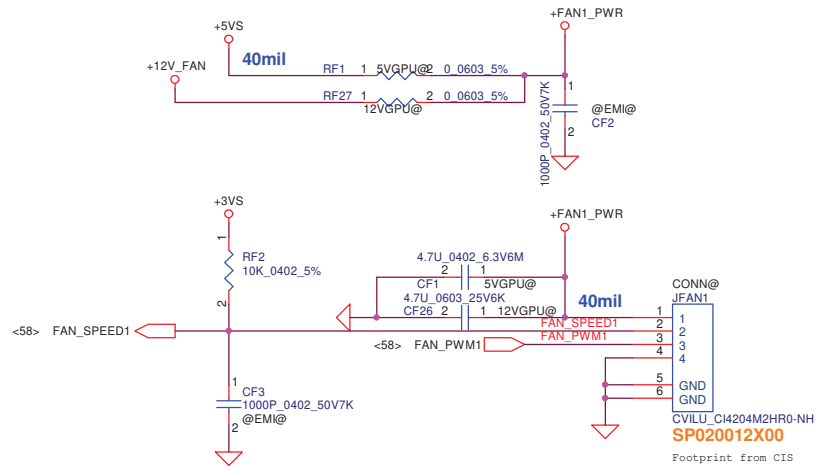
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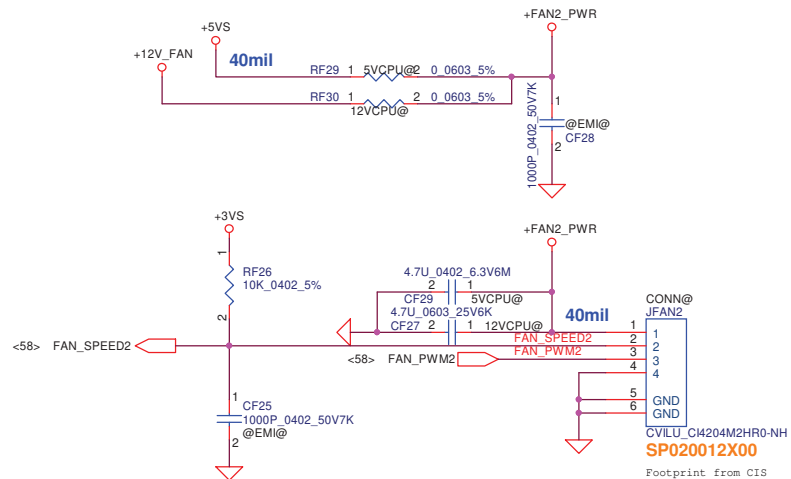
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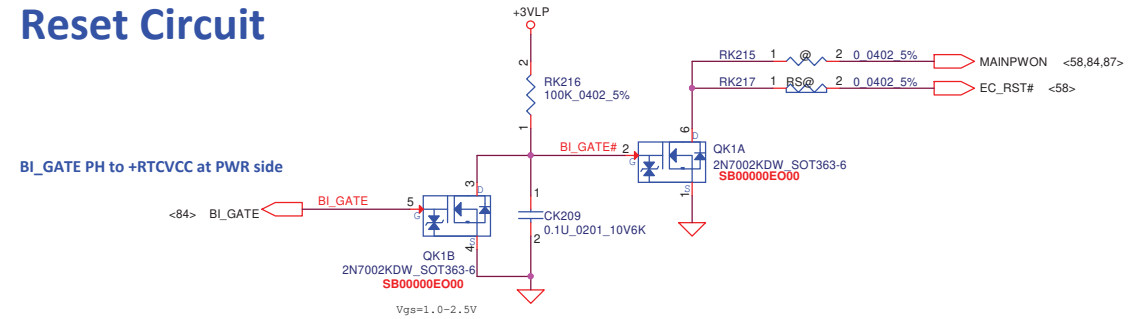
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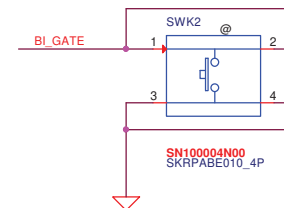
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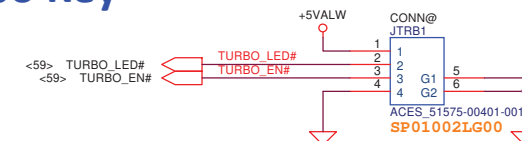
## Reset Circuit



### Reset Button



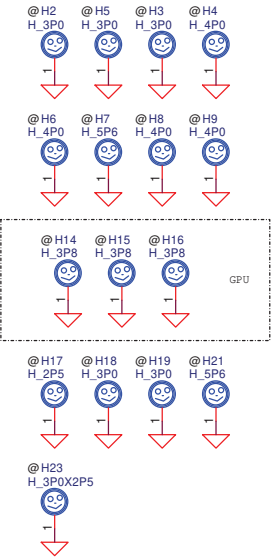
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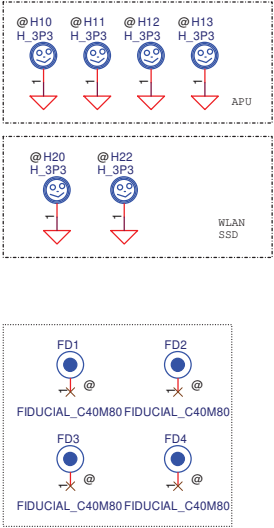
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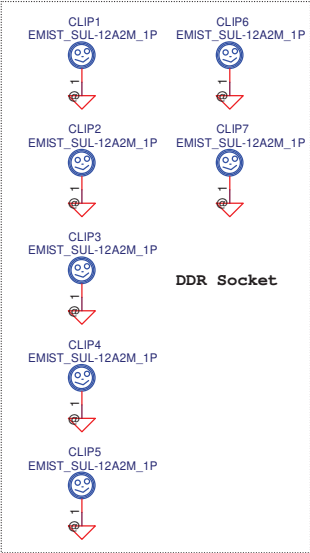
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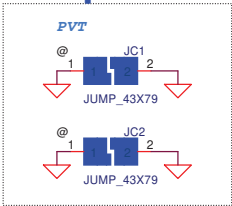
# Stand OFF



# CLIP



# Jumper for LED



ZZZ 45@  
ROYALTY HDMI W/LOGO+HDCP  
RO0000003HM

ZZZ PCB@  
PCB 3BL LA-L031P REV0 MB 4 S  
DAB0008M01A

ZZZ DAZ@  
PCB 3BL LA-L031P REV0 MB 4 S  
DAZ3BL00101

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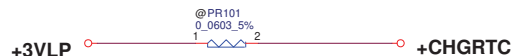
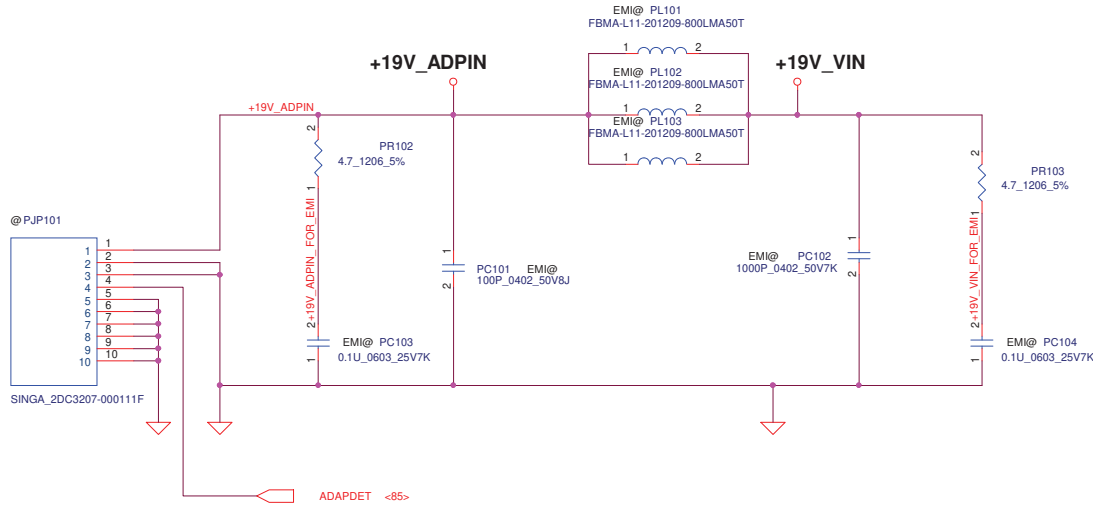
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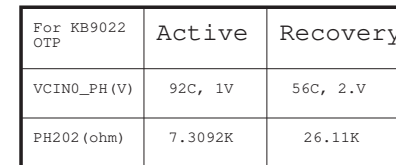
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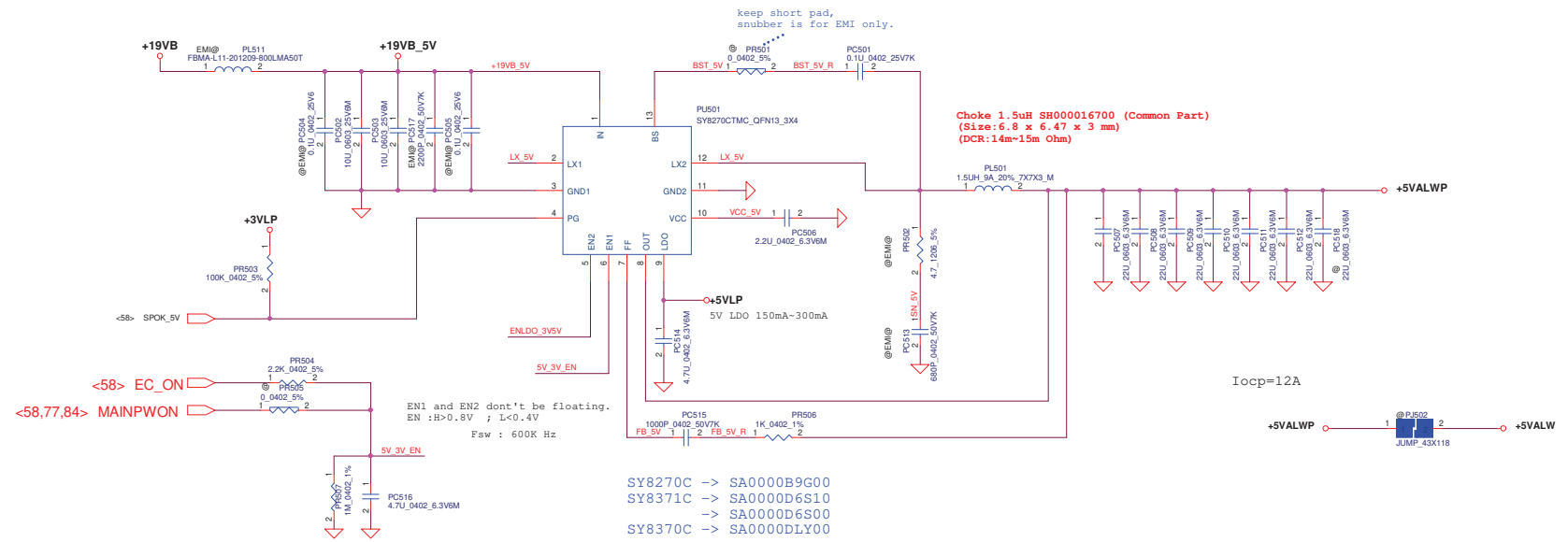
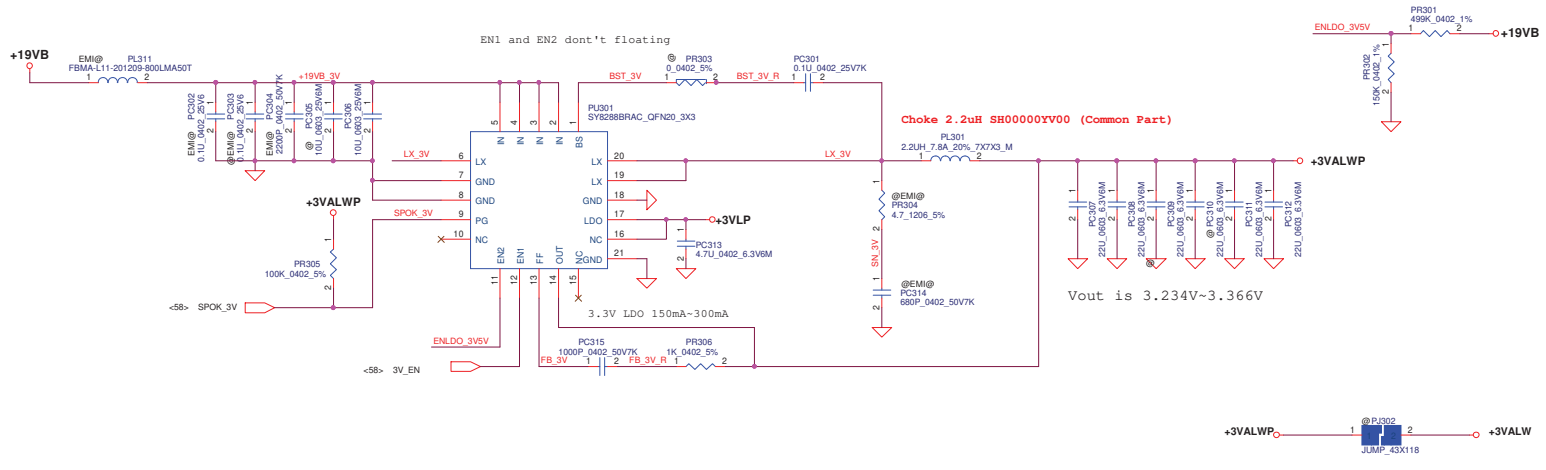
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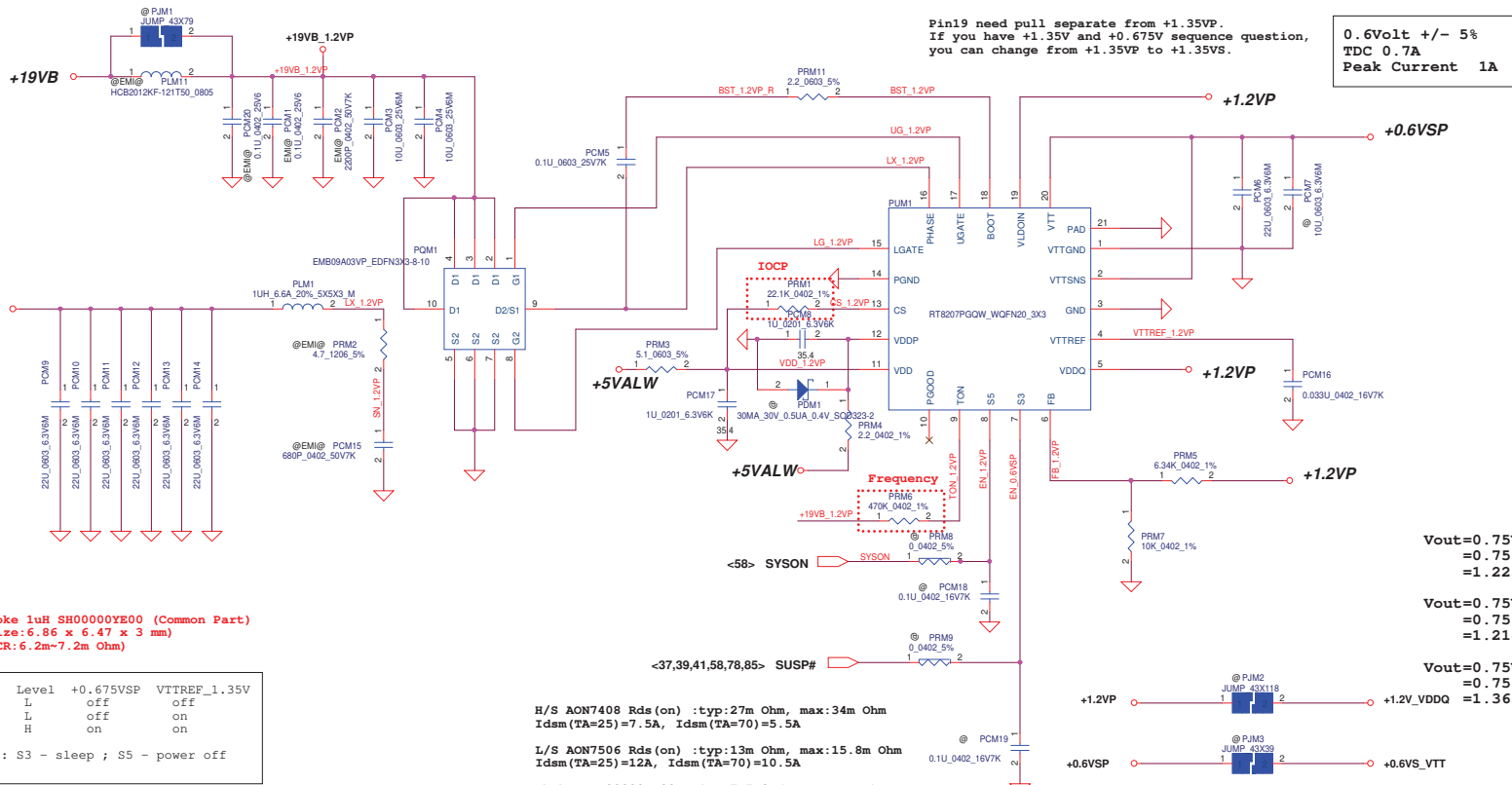
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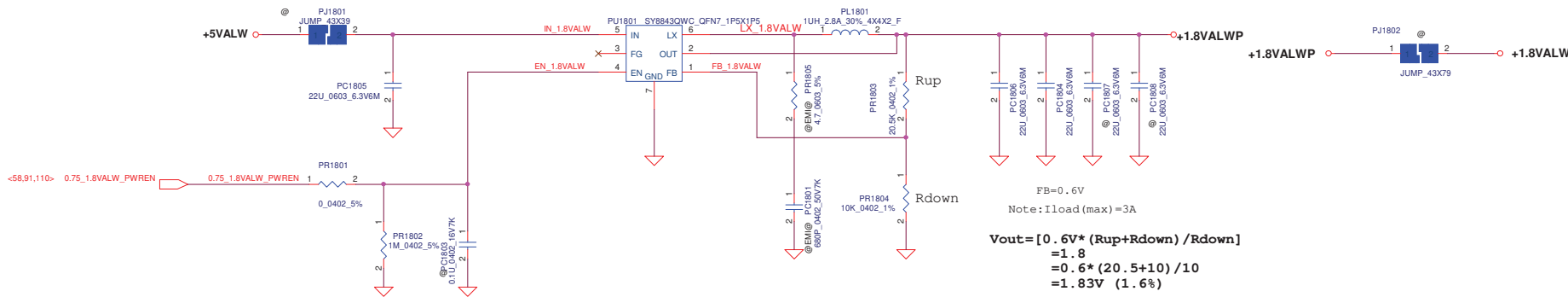
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PUM1 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%  
TDC 0.7A  
Peak Current 1A



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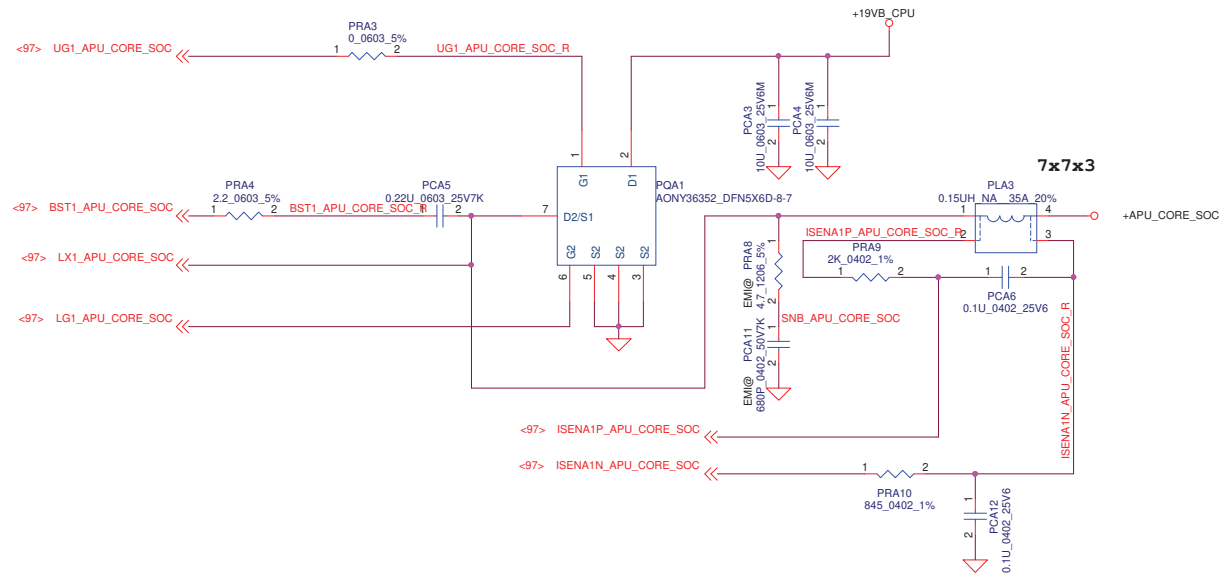
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### +APU\_CORE\_SOC

TDC 15A (45W & 54W)  
EDC 20A (45W & 54W)

TDC 13A (25W)  
EDC 17A (25W)

OCp current 28A (45W & 54W)  
OCp current 28A (25W)

Load line -2.1mV/A  
DCR 0.9mohm +/-5%

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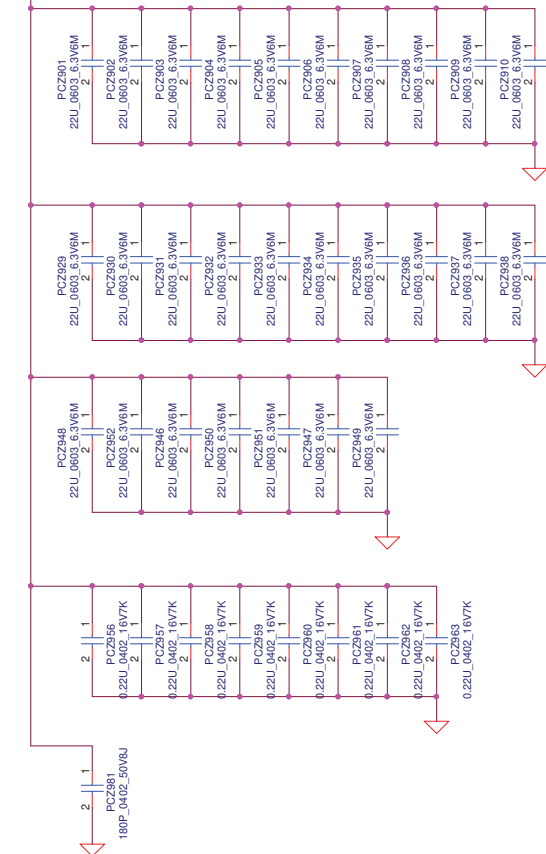
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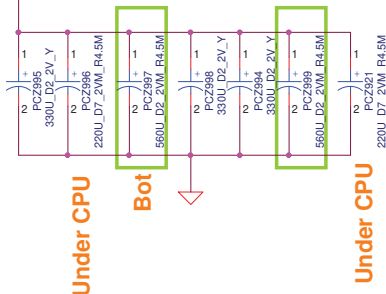


# +APU\_CORE

## +APU\_CORE



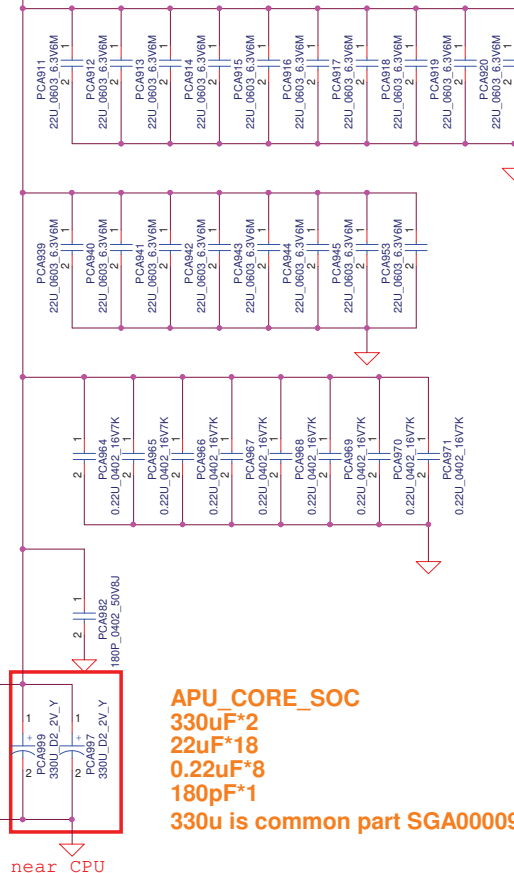
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APU\_CORE  
330uF\*5  
22uF\*27  
0.22uF\*8  
180pF\*1  
330u is common part SGA00009S00

# +APU\_CORE\_SOC

## +APU\_CORE\_SOC



APU\_CORE\_SOC  
330uF\*2  
22uF\*18  
0.22uF\*8  
180pF\*1  
330u is common part SGA00009S00

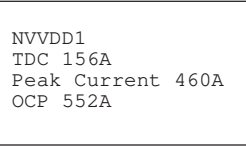
Under CPU

near CPU

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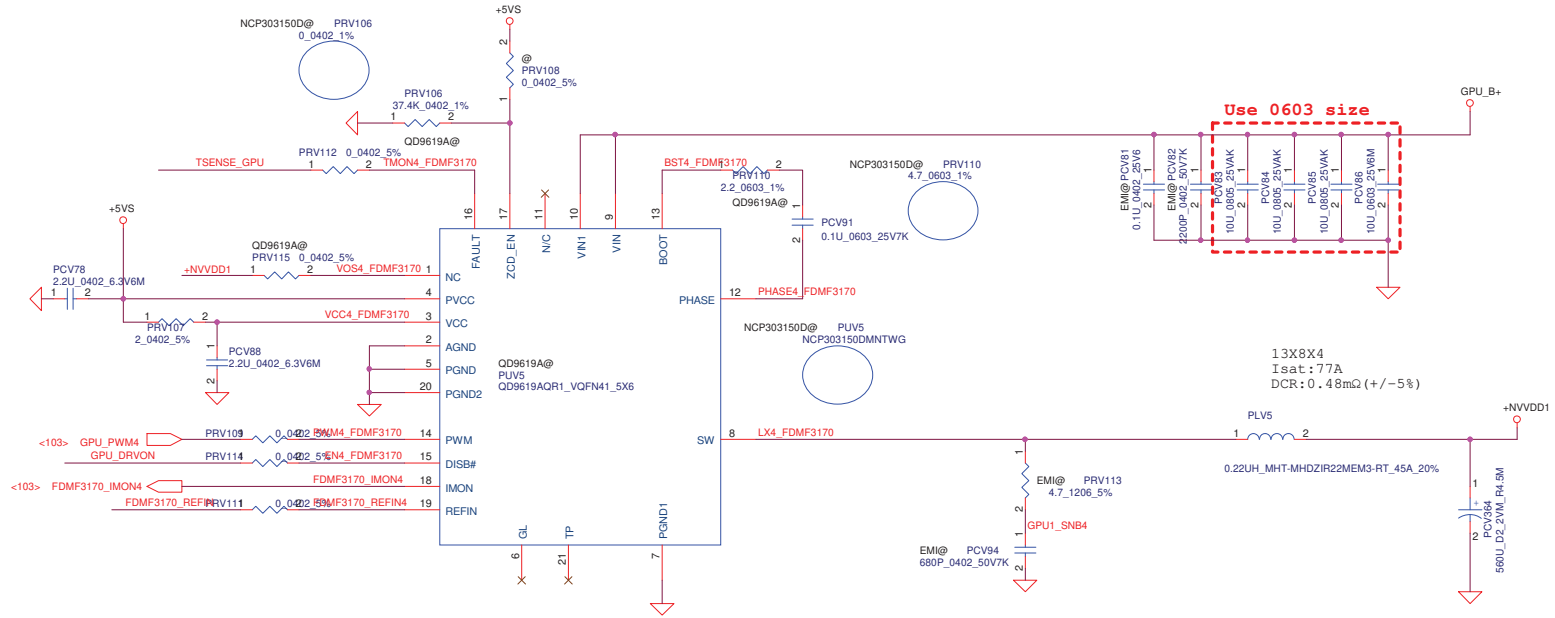
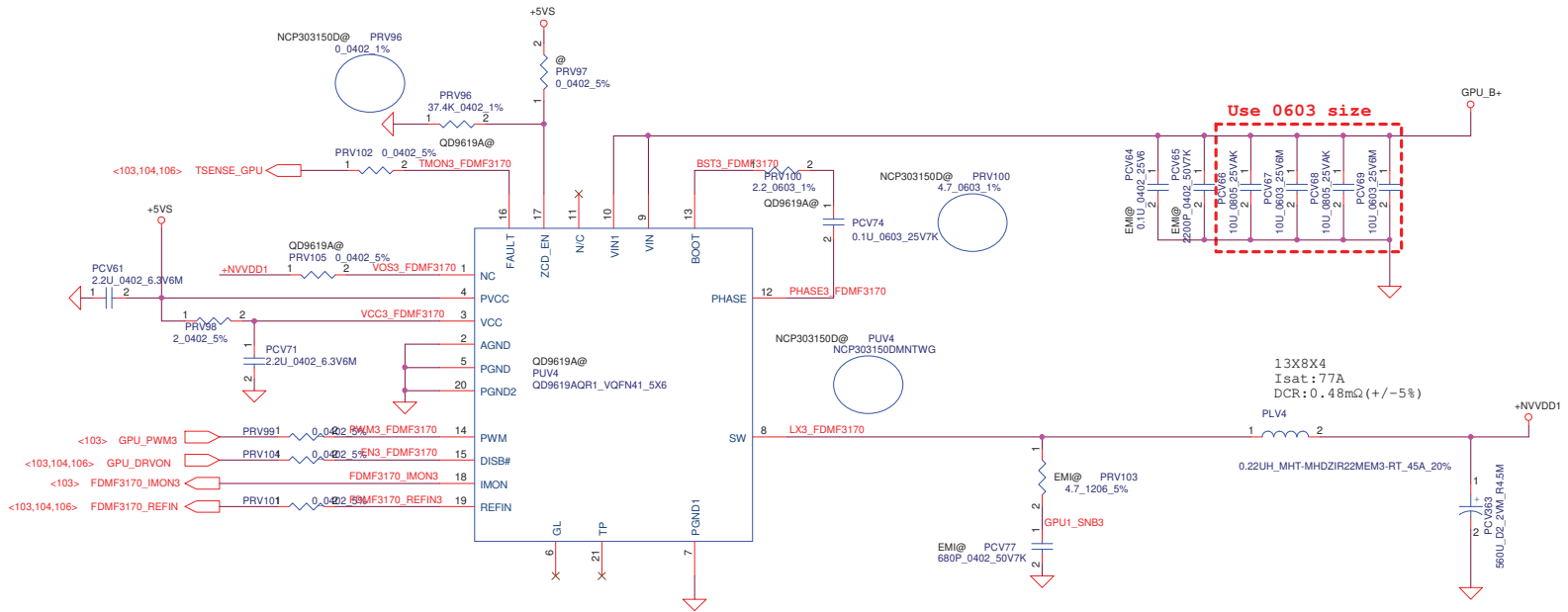
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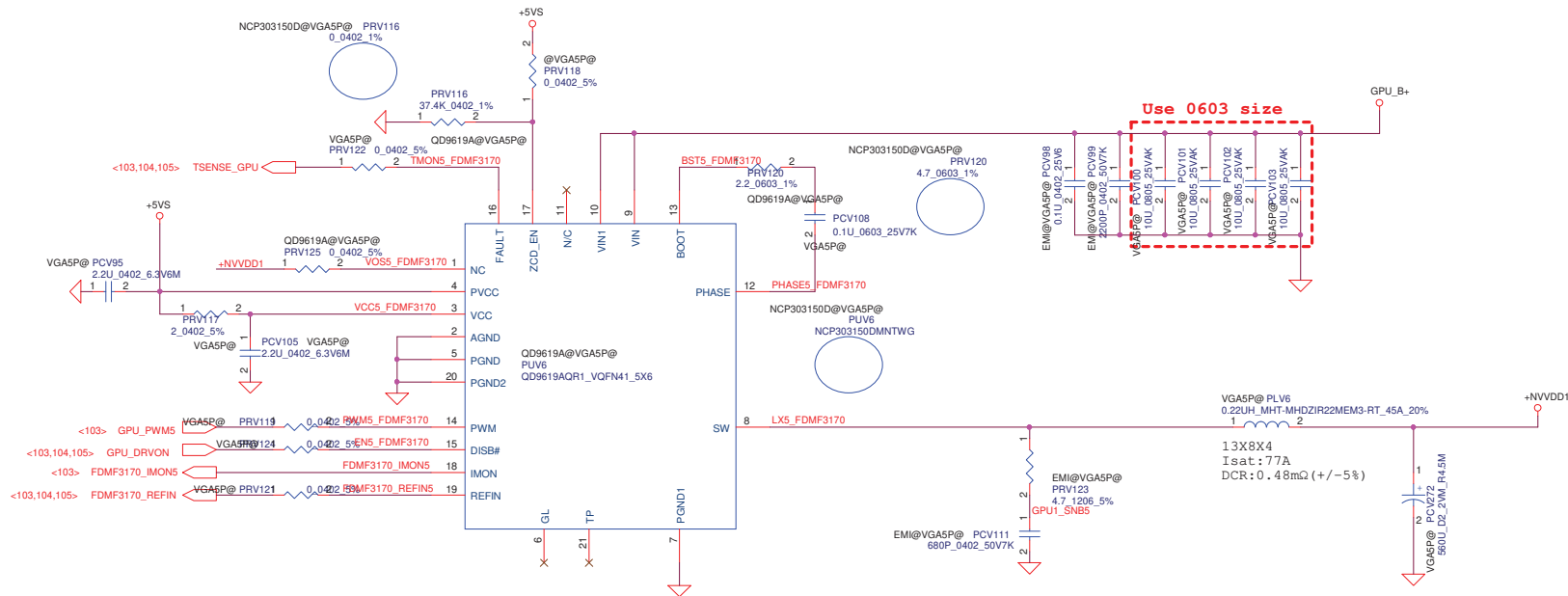
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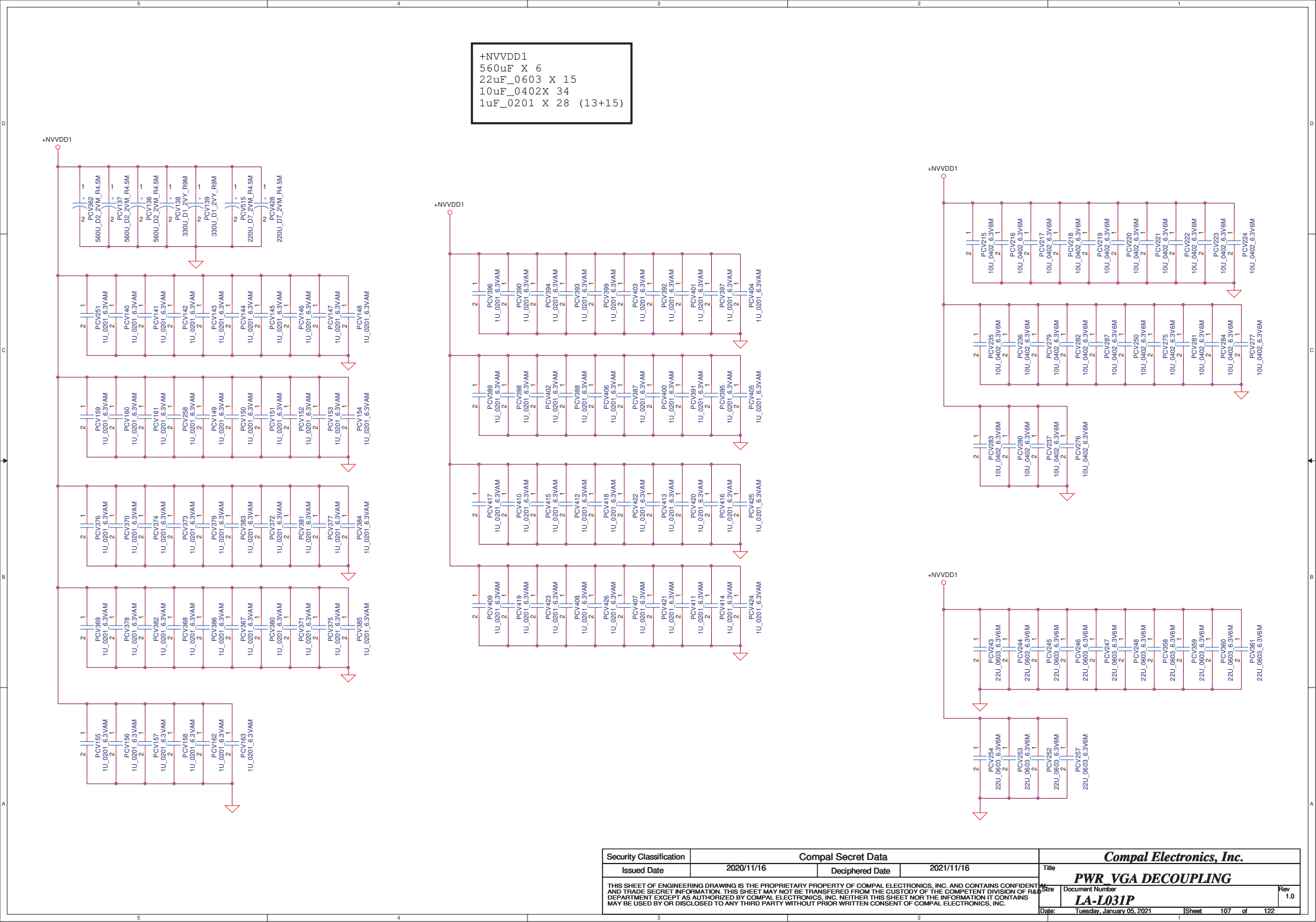


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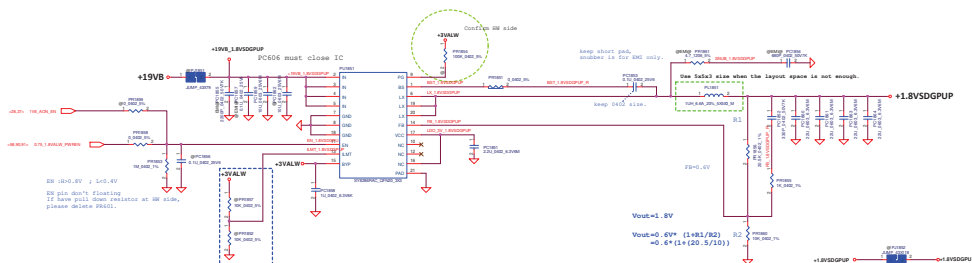
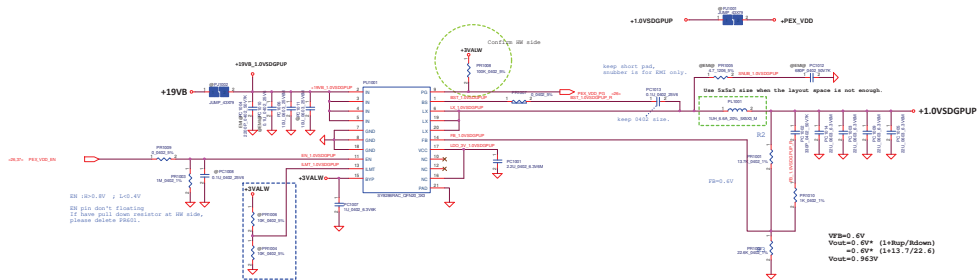






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12V FAN delete /PVT

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